User Manual

# FET6254-C, OK6254-C

ARM Cortex-A53+ ARM Cortex-M4F

Embedded Development Platform

# Hardware Manual

Rev. 1.0

July, 2022

# Update record

| Date | Manual version | SoM version | Carrier board version | Update record |
|------|----------------|-------------|------------------------|---------------|
| July, 2022 | V1.0 | V1.1 | V1.1 | First edition |

# Content

# Attentions



## MUST READ BEFORE WORKING WITH THE BOARD

Product Operation Environment:

⦿ Hot-plug of system on module and peripheral modules is strictly prohibited.

⦿ Please follow all the warnings and instructions marked on the product.

⦿ Please keep the product dry. Once splashed or immersed by any liquid, cut off the power and dry it out immediately.

⦿ Please store and operate the product in ventilating conditions to avoid damages brought by over high temperature.

⦿ Please do not use or store the product in dusty or untidy conditions.

⦿ Please do not use or store the product in alternate cold and hot conditions to avoid condensing which will damage components.

⦿ Please do not treat the product rudely. Any falling-off, knocking and violate shaking may cause destruction to circuit and components.

⦿ Please do not clean the product with organic solvents or corrodible liquids.

⦿ Please do not dismantle or repair the product by yourself. Contact us when the product malfunctions.

⦿ Please do not modify the product by yourself or use fittings unauthorized by us. Otherwise, the damage caused by that will be on your part and not included in guarantee terms.

Any questions please feel free to contact the sales engineer or Forlinx Technical Service department.

# Copyright Announcement

# Technical Support and Customization

## 1. Technical Support Range

1.1 Forlinx product related hardware and software source consulting;

1.2 Problems related to our software and hardware manual;

1.3 After-sale technical support for ODM product;

1.4 Forlinx product related trouble shooting, failure diagnose and related maintenance

## 2. Range of Technical Discussion ( non-compulsory)

2.1 Modification and comprehension of source code;

2.2 How to implant OS;

2.3 Software and hardware problems occured in self-modifying and programming

**Note:** the above three points are out of Forlinx technical service range, but Forlinx will try best but can not promise to help users to solve the problems.

## 3. Accesses to Technical Support

3.1 If you are able to understand Chinese, you can try to all the technical persons directly, the tel. number (non-instant messenger) is 0086-312-3119192

3.2 Any Forlinx product related questions or help if you need, you can send email to corresponding sales engineer whom you keep in touch with, the sales engineer will help you to follow up your issue and get back to you soonest;

3.3 If you are not able to call the technical person and don't whom you should send email to, then you can send email to our public email address sales@forlinx.com or support@forlinx.com

## 4. Access to Materials

Forlinx product related technical files will be uploaded to dropbox, when you get the board, please take your Dropbox account to create a folder and share it with Forlinx(sales@forlinx.com), Forlinx will pass the related technical files to the shared folder.

# Chapter 1 Overview of AM62x

The low-cost AM62x Sitara™ MPU family of application processors are built for Linux® application development. With scalable 64-bit Arm® Cortex®-A53 performance and embedded features, such as: dual-display support and 3D graphics acceleration, along with an extensive set of peripherals that make the AM62x device well-suited for a broad range of industrial and automotive applications while offering intelligent features and optimized power architecture as well.

The 2-port Gigabit Ethernet switch has one internal port and two external ports with Time-Sensitive Networking (TSN) support. An additional PRU module on the device enables real-time I/O capability for customer's own use cases. In addition, the extensive set of peripherals included in AM62x enables system-level connectivity, such as: USB, MMC/SD, Camera interface, OSPI, CAN-FD and GPMC for parallel host interface to an external ASIC/FPGA. The AM62x device also supports secure boot for IP protection with the built-in Hardware Security Module (HSM) and employs advanced power management support for portable and power-sensitive applications

Some of these applications include:

• Industrial HMI

• EV charging stations

• Touchless building access

• Driver monitoring systems(DMS/ OMS)/ ICM

• Retail automation

• TCU

• 3D Point Cloud

• V2X/ V2V
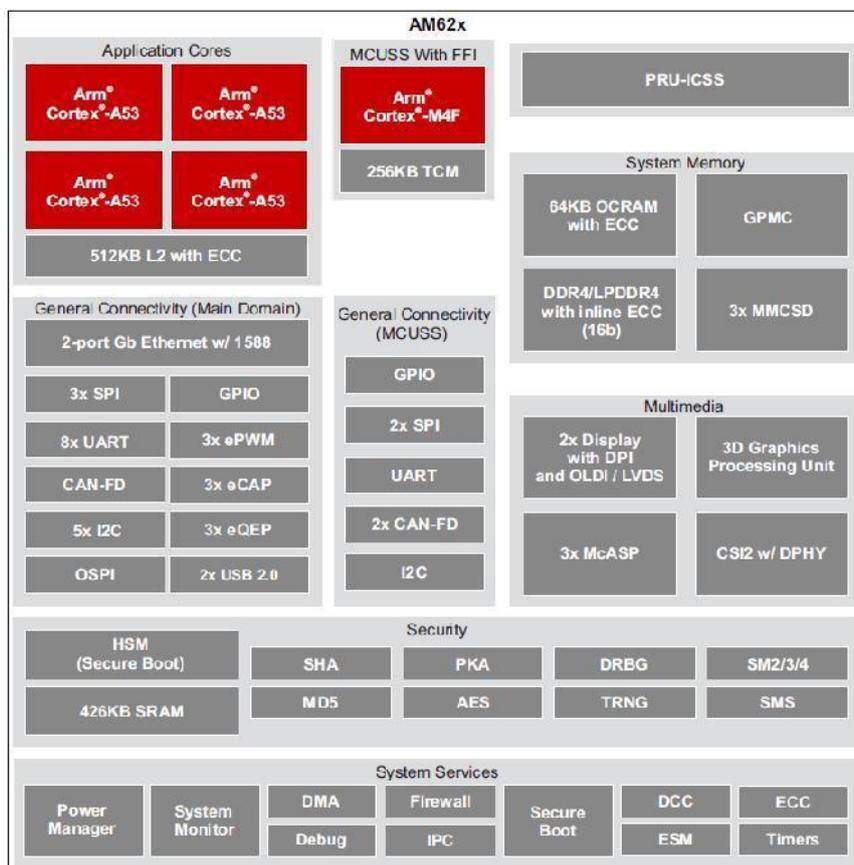
# Chapter 2 Introduction of FET6254-C SoM

## 2.1 FET6254-C Exterior
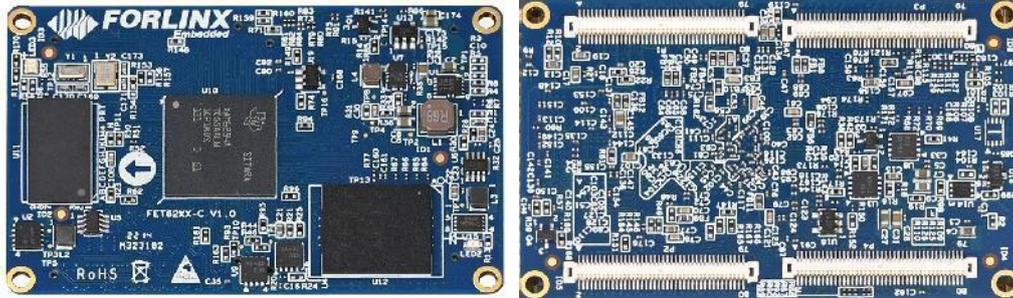


## 2.2 FET6254-C Mechanical Dimensions(Top layer+ bottom layer)
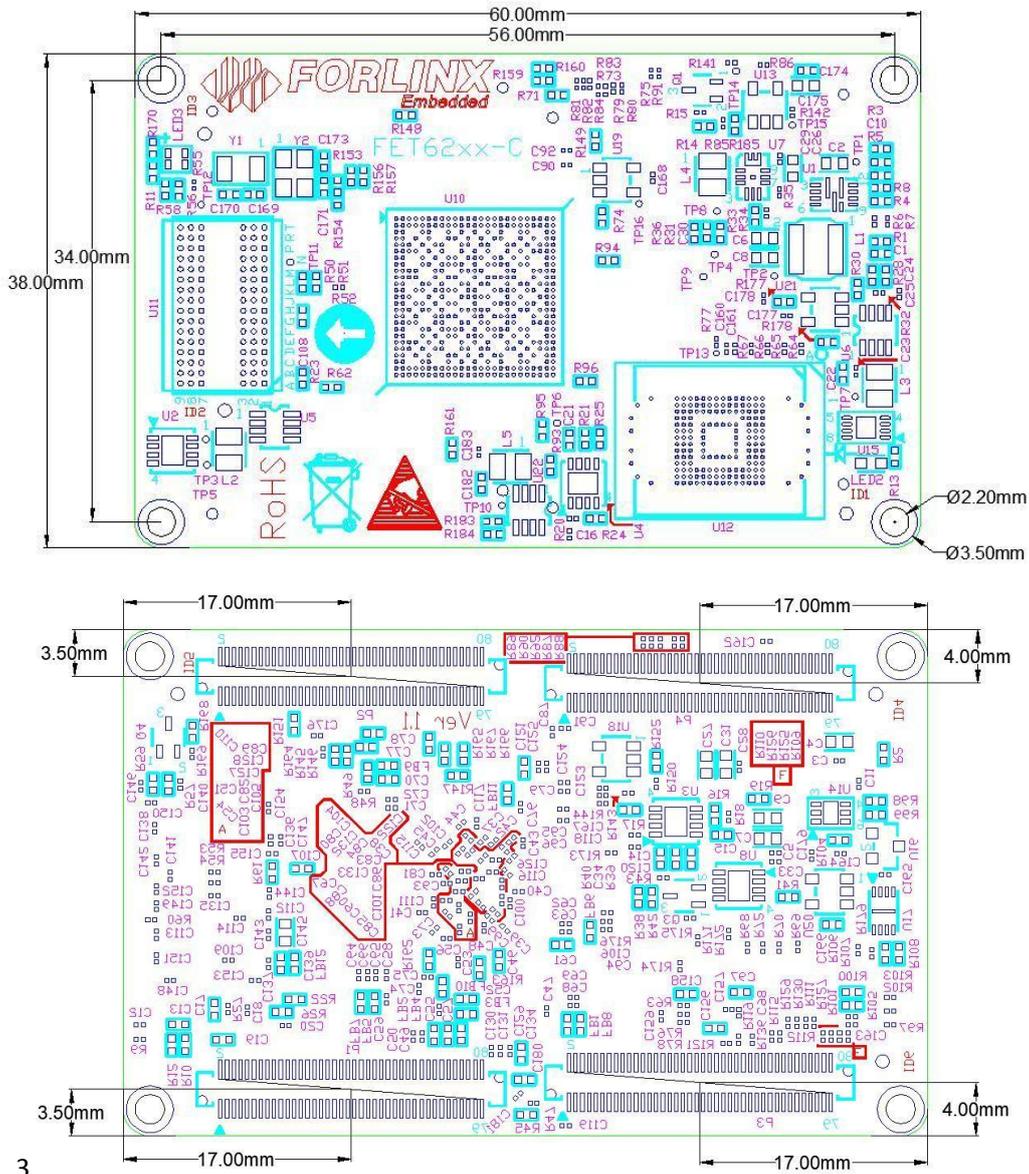
Dimensions: 60x 38mm, tolerance ±0.15mm

Processing: 1.6mm thickness, 10-layer ENIG PCB

Package: four 80-pin connectors with pitch of 0.5mm, SoM connector model is AXK6F80337YG, and mating carrier board connector model is AXK5F80537YG, about connector diagram please refer to the appendix.

The SoM is preserved with four holes with diameter of 2.2mm on its four corners which could be used for reinforcement purpose in case of vibration circumstances.

Users can take Forlinx designing for reference, use M2, L=2mm mounting nuts as below
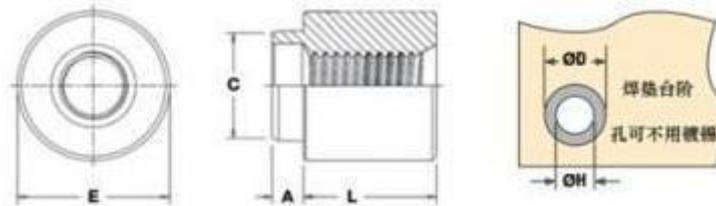


| 螺纹尺寸 | 孔深/通孔 +0.1 -0.08 | 品名 | 产品编号 | 长度 "L" ±.0.1 间隔高度 代码 | | | | 最小的板厚 | A 最大 | C 最大 | E ±0.1 | 孔 径 +0.08 | 最小焊垫 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1.8 | 2.5 | 3 | 5 | | | | | | |
| M2*0.4 | 通孔 | smtsob | M2 | 2 | 3 | 4 | 6 | 1.53 | 1.53 | 3.6 | 5.56 | 3.73 | 6.2 |

## 2.3 FET6254-C Features

### 2.3.1 Frequency

| Item | Spec. | | | | Note |
|---|---|---|---|---|---|
| | Minimum | Typical | Maximum | Unit | |
| Arm® Cortex®-53 | -- | -- | 1400 | MHz | -- |
| Arm® Cortex®-M4F | -- | -- | 400 | MHz | |
| RTC | -- | 32.768 | -- | KHz | -- |

### 2.3.2 Power Supply

| Item | Pin mark | Spec. | | | | Note |
|---|---|---|---|---|---|---|
| | | Minimum | Typical | Maximum | Unit | |
| Main power | ACIN | 4.5 | 5.0 | 5.5 | V | -- |

### 2.3.3 Working Environment

| Item | | Spec. | | | | Note |
|---|---|---|---|---|---|---|
| | | Mini | Classic | Max | Unit | |
| Temp width | Working | -40 | 25 | +85 | ℃ | Industrial grade |
| | Storage | -40 | 25 | +85 | ℃ | |
| RH | Working | 10 | -- | 90 | % RH | Non-condensing |
| | Storage | 5 | -- | 95 | % RH | |

## 2.3.4 SoM Interface Speed

| Item | Spec. | | | | Note |
|---|---|---|---|---|---|
| | Minimum | Typical | Maximum | Unit | |
| UART | — | 115200 | 3.6M | bps | -- |
| SPI | — | — | 50 | MHz | |
| IIC | — | 100 | 400 | Kbps | |
| CAN FD | — | — | 5 | Mbps | |
| USB | — | -- | 480 | Mbps | -- |

# 2.4 SoM Resource

| Peripheral | QTY | Spec. |
|---|---|---|
| LVDS[*1*2] | 2 | Two 4-lane LVDS with each lane up to 1.19Gbps;<br>A single LVDS is up to(1920 x 1200@60fps, 162MHz)<br>Can support below modes<br>Single LVDS output;<br>2x single LVDS(same content);<br>Dual LVDS output: 8-lane data and 2-lane clock combine to one display output |
| RGB Parallel | 1 | 1x 24-bit RGB parallel interface, up to WUXGA(1920x 1200@60FPS, 165MHz) |
| MIPI CSI | 1 | 1x 4-lane MIPI CSI<br>MIPI-DPHY 1.2<br>Support 1/ 2/ 3/ 4-wire mode, each up to 2.5Gbps |
| Ethernet | 2 | RMII(10/100) or RGMII(10/ 100/ 1000)<br>Supports IEEE1588(Annex D，Annex E, Annex F with 802.1AS PTP)<br>Supports TSN<br>Supports hardware IP/ UDP/ TCP verify and unload |
| USB | 2 | USB2.0 up to 480Mbps<br>Can be configured to USB host, USB device or USB dual-role device(DRD)<br>Integrated with USB VBUS |
| UART[*3] | ≤9 | Compatible with 16C750<br>Supports RS485 external transceiver auto current control<br>Rating up to 3.6Mbps baud rate<br>Supports stop-bit: 1, 1.5, 2 bit(s)<br>Parity: odd, even, none |
| SPI[*4] | ≤5 | Each lane has programmable frequency, polarity and phase serial clock<br>MCSPI is up to 50MHz |
| I2C[*5] | ≤6 | Supports standard mode(up to 100Kbps) and high speed mode(up to 400Kbps)<br>7-bit and 10-bit device addressing |
| Audio | ≤3 | Sending and receiving clock up to 50MHz<br>Supports TDM, Iner-IC Sound(I2X) and similar forms<br>Supports digital audio(SPDIF, IEC60958-1 and AES-3)<br>Supports audio reference output clock |

| ePWM | ≤3 | Each pair PWM supports two PWM output(EPWMxA and EPWMxB) applicable for below configuration<br>1. Two separate PWM output, single edge operating;<br>2. Two independent PWM outputs with bilateral symmetrical operation;<br>3. One independent PWM output with bilateral asymmetric operation,<br>4. Generated dead-band with independent rising and falling edge delay control |
|---|---|---|
| eQEP | ≤3 | Enhanced quadrature encoder pulse input<br>Supports input synchronization;<br>Supports quadrature encoder unit;<br>Supports position counters and control units for position measurement;<br>Supports quadrature edge capture unit for low-speed measurements |
| eCAP | ≤3 | Audio input sampling rate measurement;<br>Speed measurement of rotating machinery (e.g. toothed sprockets sensed by Hall sensors);<br>Elapsed time measurement between position sensor pulses;<br>Period and duty cycle measurements of pulse train signals;<br>Decode current or voltage magnitude from duty cycle encoded current/voltage sensors |
| CAN-FD[*6] | ≤3 | Complies with CAN2.0A, CAN2.0B or ISO 11898-1 protocols;<br>Supports complete CAN FD(up to 64 bytes)<br>Supports RAM parity/ ECC;<br>Rating up to 5Mbps |
| SD | ≤2 | 2x 4-bit SD/ SDIO, up to UHS-I;<br>Complies with eMMC5.1, SD3.0 and SDIO3.0 |
| GPMC | 1 | Up to 133MHz<br>Flexible 8-bit and 16-bit asynchronous memory interface, can be mounted with up to 4 chipsets(22-bit address)<br>Applicable for NAND, Nor, Muxed-Nor and SRAN |
| OSPI/ QSPI | 1 | 166MHz DDR/200MHz SDR |
| JTAG | 1 | supported |

Note:

1. Single LVDS can support WUXGA(1920x 1200@ 60p, 162MHz), it needs the receiving monitor or lin A bridge device can accept the device's video output over a single LVDS link. Generally, it's only used when display resolution less than 1366x 768. in dual-link mode, the second interface won't enlarge the band width, but reduce the required pixel cock to half.

2. Supports 1 x 2048x1080 + 1 x 1280x720;

3. 7 among the 9 UART are resource of the main domain, and the other 2 are resource of MCU domain, MCU domain names are WKUP_UART0, MCU_UART0;

4. 3 among the 5 SPI are resource of the main domain, and the other 2 are resource of MCU domain;

5. 4 among the 6 IIC are resource of the main domain, and the other 2 are resource of MCU domain;

6. 1 among 3 CAN is resouce of the main domain, and the other 2 are resource of the MCU domain

# 2.5 SoM FET6254-C Pin Definition

## 2.5.1 Schematic

P2

| Left Signal | Pin | Pin | Right Signal |
|---|---|---|---|
| | 1 | 2 | |
| MCU_GPIO0_16 | 3 | 4 | MCU_MCAN0_RX |
| MCU_GPIO0_15 | 5 | 6 | MCU_MCAN0_TX |
| | 7 | 8 | |
| MCU_UART0_TXD | 9 | 10 | WKUP_UART0_CTS |
| MCU_UART0_RXD | 11 | 12 | WKUP_UART0_RTS |
| MCU_UART0_CTS | 13 | 14 | WKUP_UART0_RX |
| MCU_UART0_RTS | 15 | 16 | WKUP_UART0_TX |
| | 17 | 18 | |
| MCU_I2C0_SCL | 19 | 20 | MCU_SPI0_CLK |
| MCU_I2C0_SDA | 21 | 22 | MCU_SPI0_D0 |
| WKUP_I2C0_SCL | 23 | 24 | MCU_SPI0_D1 |
| WKUP_I2C0_SDA | 25 | 26 | MCU_SPI0_CS0 |
| | 27 | 28 | MCU_SPI0_CS1 |
| WKUP_CLKOUT0 | 29 | 30 | |
| | 31 | 32 | SPI0_CS1 |
| MCU_SAFETY_ERRORz | 33 | 34 | SPI0_CS0 |
| CONN_MCU_PORz | 35 | 36 | SPI0_D0 |
| MCU_RESETz | 37 | 38 | SPI0_CLK |
| MCU_RESETSTATz | 39 | 40 | SPI0_D1 |
| | 41 | 42 | |
| EMU0 | 43 | 44 | UART5_RXD |
| EMU1 | 45 | 46 | UART5_TXD |
| | 47 | 48 | |
| JTAG_EMU_RSTn | 49 | 50 | SoC_I2C0_SCL |
| TRSTn | 51 | 52 | SoC_I2C0_SDA |
| TCK | 53 | 54 | I2C1_SCL |
| TMS | 55 | 56 | I2C1_SDA |
| TDI | 57 | 58 | |
| TDO | 59 | 60 | EXT_REFCLK1 |
| | 61 | 62 | |
| UART0_RXD | 63 | 64 | MCASP0_AXR0 |
| UART0_TXD | 65 | 66 | MCASP0_AXR1 |
| UART0_CTS | 67 | 68 | MCASP0_AXR2 |
| UART0_RTS | 69 | 70 | MCASP0_AXR3 |
| | 71 | 72 | MCASP0_ACLKR |
| SoC_CLKIN | 73 | 74 | MCASP0_AFSR |
| | 75 | 76 | MCASP0_AFSX |
| USB0_DRVVBUS | 77 | 78 | MCASP0_ACLKX |
| USB1_DRVVBUS | 79 | 80 | |

AXK6F80347Y

GND    GND

| | P3 | |
|---|---|---|
| | 1 | 2 |

VOUT0_VSYNC — 3
VOUT0_HSYNC — 5
VOUT0_DE — 7

CPSW_RGMII2_MDC — 11
CPSW_RGMII2_MDIO — 13

CPSW_RGMII1_RXC — 17
CPSW_RGMII1_RX_CTL — 19

CPSW_RGMII1_RD0 — 23
CPSW_RGMII1_RD1 — 25
CPSW_RGMII1_RD2 — 27
CPSW_RGMII1_RD3 — 29

CPSW_RGMII1_TXC — 33
CPSW_RGMII1_TX_CTL — 35

CPSW_RGMII1_TD0 — 39
CPSW_RGMII1_TD1 — 41
CPSW_RGMII1_TD2 — 43
CPSW_RGMII1_TD3 — 45

CPSW_RGMII2_RXC — 49
CPSW_RGMII2_RX_CTL — 51

CPSW_RGMII2_RD0 — 55
CPSW_RGMII2_RD1 — 57
CPSW_RGMII2_RD2 — 59
CPSW_RGMII2_RD3 — 61

CPSW_RGMII2_TXC — 65
CPSW_RGMII2_TX_CTL — 67

CPSW_RGMII2_TD0 — 71
CPSW_RGMII2_TD1 — 73
CPSW_RGMII2_TD2 — 75
CPSW_RGMII2_TD3 — 77

VOUT0_PCLK — 4

VOUT0_DATA0 — 10
VOUT0_DATA1 — 12
VOUT0_DATA2 — 14
VOUT0_DATA3 — 16
VOUT0_DATA4 — 18
VOUT0_DATA5 — 20
VOUT0_DATA6 — 22
VOUT0_DATA7 — 24
VOUT0_DATA8 — 28
VOUT0_DATA9 — 30
VOUT0_DATA10 — 32
VOUT0_DATA11 — 34
VOUT0_DATA12 — 36
VOUT0_DATA13 — 38
VOUT0_DATA14 — 40
VOUT0_DATA15 — 42

GPMC0_AD15 — 46
GPMC0_AD14 — 48
GPMC0_AD13 — 50
GPMC0_AD12 — 52
GPMC0_AD11 — 54
GPMC0_AD10 — 56
GPMC0_AD9 — 58
GPMC0_AD8 — 60

GPMC0_AD7 — 64
GPMC0_AD6 — 66
GPMC0_AD5 — 68
GPMC0_AD4 — 70
GPMC0_AD3 — 72
GPMC0_AD2 — 74
GPMC0_AD1 — 76
GPMC0_AD0 — 78

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GND                GND

## 2.5.2 SoM FET6254-C Pins Spec.

**Note**

| Subscript | Spec. |
|---|---|
| [1] | PIN can be configured to interrupt |
| [2] | The default power is 1.8V |
| [3] | PINs are related to CPU boot, not recommended to be used as IO. |
| [4] | Dedicated PIN, cannot be used as IO |

**Table 1 LEFT_UP (P1 ) connector pins (odd)**

| NUM | BALL | Signal name | GPIO | VOL | Pin description | Default function |
|---|---|---|---|---|---|---|
| 1 | - | GND | - | - | Ground | GND |
| 3 | - | CH1_LVDS_A0P | - | - | CH1_LVDS data A0+ | CH1_LVDS_A0P |
| 5 | - | CH1_LVDS_A0N | - | - | CH1_LVDS data A0- | CH1_LVDS_A0N |
| 7 | - | GND | - | - | Ground | GND |
| 9 | - | CH1_LVDS_A1P | - | - | CH1_LVDS data A1+ | CH1_LVDS_A1P |
| 11 | - | CH1_LVDS_A1N | - | - | CH1_LVDS data A1- | CH1_LVDS_A1N |
| 13 | - | GND | - | - | Ground | GND |
| 15 | - | CH1_LVDS_A2P | - | - | CH1_LVDS data A2+ | CH1_LVDS_A2P |
| 17 | - | CH1_LVDS_A2N | - | - | CH1_LVDS data A2- | CH1_LVDS_A2N |
| 19 | - | GND | - | - | Ground | GND |
| 21 | - | CH1_LVDS_CLKP | - | - | CH1_LVDS clock + | CH1_LVDS_CLKP |
| 23 | - | CH1_LVDS_CLKN | - | - | CH1_LVDS clock- _ | CH1_LVDS_CLKN |
| 25 | - | GND | - | - | Ground | GND |
| 27 | - | CH1_LVDS_A3P | - | - | CH1_LVDS data A3+ | CH1_LVDS_A3P |
| 29 | - | CH1_LVDS_A3N | - | - | CH1_LVDS data A3- | CH1_LVDS_A3N |
| 31 | - | GND | - | - | Ground | GND |
| 33 | - | CH2_LVDS_CLKN | - | - | CH2_LVDS clock- _ | CH2_LVDS_CLKN |
| 35 | - | CH2_LVDS_CLKP | - | - | CH2_LVDS clock + | CH2_LVDS_CLKP |
| 37 | - | GND | - | - | Ground | GND |
| 39 | - | CH2_LVDS_A1N | - | - | CH2_LVDS data A1- | CH2_LVDS_A1N |
| 41 | - | CH2_LVDS_A1P | - | - | CH2_LVDS data A1+ | CH2_LVDS_A1P |
| 43 | - | GND | - | - | Ground | GND |
| 45 | - | CH2_LVDS_A2N | - | - | CH2_LVDS data A2- | CH2_LVDS_A2N |
| 47 | - | CH2_LVDS_A2P | - | - | CH2_LVDS data A2+ | CH2_LVDS_A2P |
| 49 | - | GND | - | - | Ground | GND |
| 51 | - | CH2_LVDS_A0P | - | - | CH2_LVDS data A0+ | CH2_LVDS_A0P |
| 53 | - | CH2_LVDS_A0N | - | - | CH2_LCDS data A0- | CH2_LVDS_A0N |
| 55 | - | GND | - | - | Ground | GND |
| 57 | - | CH2_LVDS_A3P | - | - | CH2_LVDS data A3+ | CH2_LVDS_A3P |
| 59 | - | CH2_LVDS_A3N | - | - | CH2_LVDS data A3- | CH2_LVDS_A3N |
| 61 | - | GND | - | - | Ground | GND |
| 63 | - | GND | - | - | Ground | GND |
| 65 | - | USB1_DP | - | - | USB1 Data + | USB1_DP |
| 67 | - | USB1_DM | - | - | USB1 data- _ | USB1_DM |
| 69 | - | GND | - | - | Ground | GND |
| 71 | - | GND | - | - | Ground | GND |
| 73 | - | USB0_DP | - | - | USB0 data + | USB0_DP |
| 75 | - | USB0_DM | - | - | USB0 data- _ | USB0_DM |
| 77 | - | GND | - | - | Ground | GND |

| 79 | - | GND | - | - | Ground | GND |

**Table 2 LEFT_UP (P1 ) connector pins (even)**

| Num | Ball | Signal | GPIO | Vol | Spec. | Default function |
|-----|------|--------|------|-----|-------|------------------|
| 2 | - | GND | - | - | Ground | GND |
| 4 | - | CSI0_RXCLKP | - | - | MIPI_CSI0 receive clock + | CSI0_RXCLKP |
| 6 | - | CSI0_RXCLKN | - | - | MIPI_CSI0 receive clock - | CSI0_RXCLKN |
| 8 | - | GND | - | - | Ground | GND |
| 10 | - | CSI0_RXP3 | - | - | MIPI_CSI0 receive data 3+ | CSI0_RXP3 |
| 12 | - | CSI0_RXN3 | - | - | MIPI_CSI0 receive data 3- | CSI0_RXN3 |
| 14 | - | GND | - | - | Ground | GND |
| 16 | - | CSI0_RXP1 | - | - | MIPI_CSI0 receive data 1+ | CSI0_RXP1 |
| 18 | - | CSI0_RXN1 | - | - | MIPI_CSI0 receive data 1- | CSI0_RXN1 |
| 20 | - | GND | - | - | Ground | GND |
| 22 | - | CSI0_RXP2 | - | - | MIPI_CSI0 receive data 2+ | CSI0_RXP2 |
| 24 | - | CSI0_RXN2 | - | - | MIPI_CSI0 receive data 2- | CSI0_RXN2 |
| 26 | - | GND | - | - | Ground | GND |
| 28 | - | CSI0_RXP0 | - | - | MIPI_CSI0 receive data 0+ | CSI0_RXP0 |
| 30 | - | CSI0_RXN0 | - | - | MIPI_CSI0 receive data 0- | CSI0_RXN0 |
| 32 | - | GND | - | - | Ground | GND |
| 34 | - | GND | - | - | Ground | GND |
| 36 | - | GND | - | - | Ground | GND |
| 38 | - | GND | - | - | Ground | GND |
| 40 | - | GND | - | - | Ground | GND |
| 42 | - | GND | - | - | Ground | GND |
| 44 | - | GND | - | - | Ground | GND |
| 46 | - | GND | - | - | Ground | GND |
| 48 | - | GND | - | - | Ground | GND |
| 50 | - | GND | - | - | Ground | GND |
| 52 | - | GND | - | - | Ground | GND |
| 54 | - | GND | - | - | Ground | GND |
| 56 | - | GND | - | - | Ground | GND |
| 58 | - | GND | - | - | Ground | GND |
| 60 | - | GND | - | - | Ground | GND |
| 62 | - | GND | - | - | Ground | GND |
| 64 | - | GND | - | - | Ground | GND |
| 66 | - | GND | - | - | Ground | GND |
| 68 | - | GND | - | - | Ground | GND |
| 70 | - | USB0_VBUS | - | 1.8 | USB0_VBUS detection | USB0_VBUS |
| 72 | - | GND | - | - | Ground | GND |
| 74 | - | GND | - | - | Ground | GND |
| 76 | - | USB1_VBUS | - | 1.8 | USB1_VBUS detection | USB1_VBUS |
| 78 | - | GND | - | - | Ground | GND |
| 80 | - | GND | - | - | Ground | GND |

**Table 3 RIGHT_UP （P2 ） pins (odd)**

| Num | Ball | Signal | GPIO | Vo l | Spec. | Default function |
|---|---|---|---|---|---|---|
| 1 | - | GND | - | - | Ground | GND |
| 3 | D4 | MCU_GPIO0_16 | MCU | 3.3 | MCU domain GPIO0_16 | MCU_GPIO0_16 |
| 5 | E5 | MCU_GPIO0_15 | MCU | 3.3 | MCU domain GPIO0_15 | MCU_GPIO0_15 |
| 7 | - | GND | - | - | Ground | GND |
| 9 | A5 | MCU_UART0_TXD | MCU | 3.3 | MCU domain UART0 send | MCU_UART0_TXD |
| 11 | B5 | MCU_UART0_RXD | MCU | 3.3 | MCU domain UART0 | MCU_UART0_RXD |
| 13 | A6 | | MCU | 3.3 | MCU domain UART0 clear | |
| 15 | B6 | MCU_UART0_RTS | MCU | 3.3 | MCU domain UART0 | MCU_GPIO0_8 |
| 17 | - | GND | - | - | Ground | GND |
| 19 | A8 | MCU_I2C0_SCL | MCU | 3.3 | MCU domain I2C0 clock | MCU_I2C0_SCL |
| 21 | D1 | MCU_I2C0_SDA | MCU | 3.3 | MCU domain I2C0 data | MCU_I2C0_SDA |
| 23 | B9 | WKUP_I2C0_SCL | MCU | 3.3 | WKUP domain I2C0 clock | WKUP_I2C0_SCL |
| 25 | A9 | WKUP_I2C0_SDA | MCU | 3.3 | WKUP domain I2C0 data | WKUP_I2C0_SDA |
| 27 | - | GND | - | - | Ground | GND |
| 29 | A1 | WKUP_CLKOUT0 | MCU | 3.3 | WKUP domain CLKOUT0 | WKUP_CLKOUT0 |
| 31 | - | GND | - | - | Ground | GND |
| 33 | - | | - | 1.8 | MCU domain ESM error | MCU_SAFETY_ERROR |
| 35 | - | CONN_MCU_POR | - | 3.3 | MCU domain cold reset | CONN_MCU_PORZ |
| 37 | - | MCU_RESETZ | - | 3.3 | MCU domain warm reset | MCU_RESETZ |
| 39 | - | MCU_RESETSTATZ TZ | - | 3.3 V | MCU domain warm reset output | MCU_RESETSTATZ |
| 41 | - | GND | - | - | Ground | GND |
| 43 | - | EMU0 | - | 3.3 | Simulation Control 0 | EMU0 |
| 45 | - | EMU1 | - | 3.3 | Simulation Control 1 | EMU1 |
| 47 | - | GND | - | - | Ground | GND |
| 49 | - | JTAG_EMU_RSTN | - | 3.3 | JTAG_EMU cold reset | JTAG_EMU_RSTN |
| 51 | B1 | TRSTN | - | 3.3 | JTAG reset | TRSTN |
| 53 | A1 | TCK | - | 3.3 | JTAG test clock input | TCK |
| 55 | B1 | TMS | - | 3.3 | JTAG test mode select input | TMS |
| 57 | A1 | TDI | - | 3.3 | JTAG test data input | TDI |
| 59 | D1 | TDO | - | 3.3 | JTAG test data output | TDO |
| 61 | - | GND | - | - | Ground | GND |
| 63 | D1 | UART0_RXD | GPIO1 | 3.3 | main domain UART0 | UART0_RXD |
| 65 | E1 | UART0_TXD | GPIO1 | 3.3 | main domain UART0 | UART0_TXD |
| 67 | A1 | | GPIO1 | 3.3 | main domain UART0 clear | |
| 69 | B1 | | GPIO1 | 3.3 | main domain UART0 | |
| 71 | - | GND | - | - | Ground | GND |
| 73 | - | SOC_CLKIN | - | 1.8 | SoM clock input (default | SOC_CLKIN |
| 75 | - | GND | - | - | Ground | GND |
| 77 | - | USB0_DRVVBUS | - | 3.3 | USB0 VBUS control output | USB0_DRVVBUS |
| 79 | - | USB1_DRVVBUS | - | 3.3 | USB1 VBUS control output | USB1_DRVVBUS |

**Table 4 RIGHT UP (P2) (even)**

| Num | Ball | Signal | GPIO | Vol | Spec. | Default function |
|---|---|---|---|---|---|---|
| 2 | - | GND | - | - | Ground | GND |
| 4 | B3 | MCU MCAN | MCU GPIO | 3.3 | MCU domain CAN0 | MCU MCAN0 RX |
| 6 | D6 | MCU MCAN | MCU GPIO | 3.3 | MCU domain CAN0 | MCU MCAN0 TX |
| 8 | - | GND | - | - | Ground | GND |
| 10 | C6 | WKUP UAR | MCU GPIO | 3.3 | WKUP domain UART0 | MCU GPIO0 11 |
| 12 | A4 | WKUP UAR | MCU GPIO | 3.3 | WKUP domain UART0 | MCU GPIO0 12 |
| 14 | B4 | WKUP UAR | MCU GPIO | 3.3 | WKUP domain UART0 | WKUP UART0 RX |
| 16 | C5 | WKUP UAR | MCU GPIO | 3.3 | WKUP domain UART0 | WKUP UART0 TX |
| 18 | - | GND | - | - | Ground | GND |
| 20 | A7 | MCU SPI0 C | MCU GPIO | 3.3 | MCU domain SPI0 clock | MCU SPI0 CLK |
| 22 | D9 | MCU_SPI0_D0 | MCU_GPIO0_3 | 3.3V | MCU domain SPI0 data 0 | MCU_SPI0_D0 |
| 24 | C9 | MCU SPI0 D | MCU GPIO | 3.3 | MCU Domain SPI0 Data 1 | MCU SPI0 D1 |
| 26 | E8 | MCU SPI0 C | MCU GPIO | 3.3 | MCU domain SPI0 chip | MCU SPI0 CS0 |
| 28 | B8 | MCU SPI0 C | MCU GPIO | 3.3 | MCU domain SPI0 chip | MCU SPI0 CS1 |
| 30 | - | GND | - | - | Ground | GND |
| 32 | C13 | SPI0 CS1 | GPIO1 16 | 3.3 | main domain SPI0 chip | GPIO1 16 |
| 34 | A13 | SPI0 CS0 | GPIO1 15 | 3.3 | main domain SPI0 chip | GPIO1 15 |
| 36 | B13 | SPI0 D0 | GPIO1 18 | 3.3 | main domain SPI0 data 0 | GPIO1 18 |
| 38 | A14 | SPI0 CLK | GPIO1 17 | 3.3 | main domain SPI0 clock | GPIO1 17 |
| 40 | B14 | SPI0 D1 | GPIO1 19 | 3.3 | main domain SPI0 data 1 | GPIO1 19 |
| 42 | - | GND | - | - | Ground | GND |
| 44 | C15 | UART5 RXD | GPIO1 24 | 3.3 | main domain UART5 | UART5 RXD |
| 46 | E15 | UART5 TXD | GPIO1 25 | 3.3 | main domain UART5 | UART5 TXD |
| 48 | - | GND | - | - | Ground | GND |
| 50 | B16 | SOC I2C0 S | GPIO1 26 | 3.3 | main domain I2C0 clock | SOC I2C0 SCL |
| 52 | A16 | SOC I2C0 S | GPIO1 27 | 3.3 | main domain I2C0 data | SOC I2C0 SDA |
| 54 | B17 | I2C1 SCL | GPIO1 28 | 3.3 | main domain I2C1 clock | I2C1 SCL |
| 56 | A17 | I2C1 SDA | GPIO1 29 | 3.3 | main domain I2C1 data | I2C1 SDA |
| 58 | - | GND | - | - | Ground | GND |
| 60 | - | EXT REFCL | - | 3.3 | External clock input to | EXT REFCLK1 |
| 62 | - | GND | - | - | Ground | GND |
| 64 | E18 | MCASP0 AX | GPIO1 10 | 3.3 | MCASP0 Serial Data 0 | LCD PWM |
| 66 | B18 | MCASP0 AX | GPIO1 9 | 3.3 | MCASP0 Serial Data 1 | LVDS PWM |
| 68 | A19 | MCASP0 AX | GPIO1 8 | 3.3 | MCASP0 Serial Data 2 | MCASP0 AXR2 |
| 70 | B19 | MCASP0 AX | GPIO1 7 | 3.3 | MCASP0 Serial Data 3 | MCASP0 AXR3 |
| 72 | A20 | MCASP0 AC | GPIO1 14 | 3.3 | MCASP0 receive bit | MCASP0 ACLKR |
| 74 | E19 | MCASP0 AF | GPIO1 13 | 3.3 | MCASP0 receive frame | MCASP0 AFSR |
| 76 | D20 | MCASP0 AF | GPIO1 12 | 3.3 | MCASP0 transmit bit | MCASP0 AFSX |
| 78 | B20 | MCASP0 AC | GPIO1 11 | 3.3 | MCASP0 transmit frame | MCASP0 ACLKX |
| 80 | - | GND | - | - | Ground | GND |

**Table 5 LEFT_DOWN (P3 ) (odd)**

| Num | Ball | Signal | GPIO | Vol | Spec. | Default function |
|---|---|---|---|---|---|---|
| 1 | - | GND | - | - | Ground | GND |
| 3 | AC25 | VOUT0_VSYNC | GPIO0_63 | 3.3V | Video output vertical sync | VOUT0_VSYNC |
| 5 | AB24 | VOUT0_HSYNC | GPIO0_61 | 3.3V | Video output horizontal sync | VOUT0_HSYNC |
| 7 | Y20 | VOUT0_DE | GPIO0_62 | 3.3V | Video output data enable | VOUT0_DE |
| 9 | - | GND | - | - | Ground | GND |
| 11 | AD24 | CPSW_RGMII2_MDC | GPIO0_86 | 3.3V | MDIO clock | CPSW_RGMII2_MDC |
| 13 | AB22 | CPSW_RGMII2_MDIO | GPIO0_85 | 3.3V | MDIO data | CPSW_RGMII2_MDIO |
| 15 | - | GND | - | - | Ground | GND |
| 17 | AD17 | CPSW_RGMII1_RXC | GPIO0_80 | 3.3V | RGMII1 receive clock | CPSW_RGMII1_RXC |
| 19 | AE17 | CPSW_RGMII1_RX_CTL | GPIO0_79 | 3.3V | RGMII1 receive control | CPSW_RGMII1_RX_CTL |
| 21 | - | GND | - | - | Ground | GND |
| 23 | AB17 | CPSW_RGMII1_RD0 | GPIO0_81 | 3.3V | RGMII1 receive data 0 | CPSW_RGMII1_RD0 |
| 25 | AC17 | CPSW_RGMII1_RD1 | GPIO0_82 | 3.3V | RGMII1 receive data 1 | CPSW_RGMII1_RD1 |
| 27 | AB16 | CPSW_RGMII1_RD2 | GPIO0_83 | 3.3V | RGMII1 receive data 2 | CPSW_RGMII1_RD2 |
| 29 | AA15 | CPSW_RGMII1_RD3 | GPIO0_84 | 3.3V | RGMII1 receive data 3 | CPSW_RGMII1_RD3 |
| 31 | - | GND | - | - | Ground | GND |
| 33 | AE19 | CPSW_RGMII1_TXC | GPIO0_74 | 3.3V | RGMII1 transmit clock | CPSW_RGMII1_TXC |
| 35 | AD19 | CPSW_RGMII1_TX_CTL | GPIO0_73 | 3.3V | RGMII1 transmit control | CPSW_RGMII1_TX_CTL |
| 37 | - | GND | - | - | Ground | GND |
| 39 | AE20 | CPSW_RGMII1_TD0 | GPIO0_75 | 3.3V | RGMII1 transmit data 0 | CPSW_RGMII1_TD0 |
| 41 | AD20 | CPSW_RGMII1_TD1 | GPIO0_76 | 3.3V | RGMII1 transmit data 1 | CPSW_RGMII1_TD1 |
| 43 | AE18 | CPSW_RGMII1_TD2 | GPIO0_77 | 3.3V | RGMII1 transmit data 2 | CPSW_RGMII1_TD2 |
| 45 | AD18 | CPSW_RGMII1_TD3 | GPIO0_78 | 3.3V | RGMII1_transmit data 3 | CPSW_RGMII1_TD3 |
| 47 | - | GND | - | - | Ground | GND |
| 49 | AD23 | CPSW_RGMII2_RXC | GPIO1_2 | 3.3V | RGMII2 receive clock | CPSW_RGMII2_RXC |
| 51 | AD22 | CPSW_RGMII2_RX_CTL | GPIO1_1 | 3.3V | RGMII2 receive control | CPSW_RGMII2_RX_CTL |
| 53 | - | GND | - | - | Ground | GND |
| 55 | AE23 | CPSW_RGMII2_RD0 | GPIO1_3 | 3.3V | RGMII2 receive data 0 | CPSW_RGMII2_RD0 |
| 57 | AB20 | CPSW_RGMII2_RD1 | GPIO1_4 | 3.3V | RGMII2 receive data 1 | CPSW_RGMII2_RD1 |
| 59 | AC21 | CPSW_RGMII2_RD2 | GPIO1_5 | 3.3V | RGMII2 receive data 2 | CPSW_RGMII2_RD2 |
| 61 | AE22 | CPSW_RGMII2_RD3 | GPIO1_6 | 3.3V | RGMII2 receive data 3 | CPSW_RGMII2_RD3 |
| 63 | - | GND | - | - | Ground | GND |
| 65 | AE21 | CPSW_RGMII2_TXC | GPIO0_88 | 3.3V | RGMII2 transmit clock | CPSW_RGMII2_TXC |
| 67 | AA19 | CPSW_RGMII2_TX_CTL | GPIO0_87 | 3.3V | RGMII2 transmit control | CPSW_RGMII2_TX_CTL |
| 69 | - | GND | - | - | Ground | GND |
| 71 | Y18 | CPSW_RGMII2_TD0 | GPIO0_89 | 3.3V | RGMII2 transmit data 0 | CPSW_RGMII2_TD0 |
| 73 | AA18 | CPSW_RGMII2_TD1 | GPIO0_90 | 3.3V | RGMII2 transmit data 1 | CPSW_RGMII2_TD1 |
| 75 | AD21 | CPSW_RGMII2_TD2 | GPIO0_91 | 3.3V | RGMII2 transmit data 2 | CPSW_RGMII2_TD2 |
| 77 | AC20 | CPSW_RGMII2_TD3 | GPIO1_0 | 3.3V | RGMII2 transmit data 3 | CPSW_RGMII2_TD3 |
| 79 | - | GND | - | - | Ground | GND |

**Table 6 LEFT_DOWN (P3) (even)**

| Num | Ball | Signal | GPIO | Vol | Spec. | Default function |
|-----|------|--------|------|-----|-------|------------------|
| 2 | - | GND | - | - | Ground | GND |
| 4 | AC24 | VOUT0_PCLK | GPIO0_64 | 3.3V | Video output pixel clock | VOUT0_PCLK |
| 6 | - | GND | - | - | Ground | GND |
| 8 | - | GND | - | - | Ground | GND |
| 10 | U22 | VOUT0_DATA0 | GPIO0_45 | 3.3V | Video output data 0 | VOUT0_DATA0 |
| 12 | V24 | VOUT0_DATA1 | GPIO0_46 | 3.3V | Video output data 1 | VOUT0_DATA1 |
| 14 | W25 | VOUT0_DATA2 | GPIO0_47 | 3.3V | Video output data 2 | VOUT0_DATA2 |
| 16 | W24 | VOUT0_DATA3 | GPIO0_48 | 3.3V | Video output data 3 | VOUT0_DATA3 |
| 18 | Y25 | VOUT0_DATA4 | GPIO0_49 | 3.3V | Video output data 4 | VOUT0_DATA4 |
| 20 | Y24 | VOUT0_DATA5 | GPIO0_50 | 3.3V | Video output data 5 | VOUT0_DATA5 |
| 22 | Y23 | VOUT0_DATA6 | GPIO0_51 | 3.3V | Video output data 6 | VOUT0_DATA6 |
| 24 | AA25 | VOUT0_DATA7 | GPIO0_52 | 3.3V | Video output data 7 | VOUT0_DATA7 |
| 26 | - | GND | - | - | Ground | GND |
| 28 | V21 | VOUT0_DATA8 | GPIO0_53 | 3.3V | Video output data 8 | VOUT0_DATA8 |
| 30 | W21 | VOUT0_DATA9 | GPIO0_54 | 3.3V | Video output data9 | VOUT0_DATA9 |
| 32 | V20 | VOUT0_DATA1 | GPIO0_55 | 3.3V | Video output data 10 | VOUT0_DATA10 |
| 34 | AA23 | VOUT0_DATA11 | GPIO0_56 | 3.3V | Video output data 11 | VOUT0_DATA11 |
| 36 | AB25 | VOUT0_DATA1 | GPIO0_57 | 3.3V | Video output data 12 | VOUT0_DATA12 |
| 38 | AA24 | VOUT0_DATA1 | GPIO0_58 | 3.3V | Video output data 13 | VOUT0_DATA13 |
| 40 | Y22 | VOUT0_DATA1 | GPIO0_59 | 3.3V | Video output data 14 | VOUT0_DATA14 |
| 42 | AA21 | VOUT0_DATA1 | GPIO0_60 | 3.3V | Video output data 15 | VOUT0_DATA15 |
| 44 | - | GND | - | - | Ground | GND |
| 46 | U24 | GPMC0_AD15 | GPIO0_30 | 3.3V | GPMC Data 15/ Address 16 | GPMC0_AD15 |
| 48 | U25 | GPMC0_AD14 | GPIO0_29 | 3.3V | GPMC data 14/ address 15 | GPMC0_AD14 |
| 50 | T24 | GPMC0_AD13 | GPIO0_28 | 3.3V | GPMC data 13/ address 14 | GPMC0_AD13 |
| 52 | T22 | GPMC0_AD12 | GPIO0_27 | 3.3V | GPMC data 12/ address 13 | GPMC0_AD12 |
| 54 | R21 | GPMC0_AD11 | GPIO0_26 | 3.3V | GPMC data 11/ address 12 | GPMC0_AD11 |
| 56 | T25 | GPMC0_AD10 | GPIO0_25 | 3.3V | GPMC data 10/ address 11 | GPMC0_AD10 |
| 58 | R25 | GPMC0_AD9 | GPIO0_24 | 3.3V | GPMC Data 9/ Address 10 | GPMC0_AD9 |
| 60 | R24 | GPMC0_AD8 | GPIO0_23 | 3.3V | GPMC Data 8/ Address 9 | GPMC0_AD8 |
| 62 | - | GND | - | - | Ground | GND |
| 64 | R23 | GPMC0_AD7 | GPIO0_22 | 3.3V | GPMC Data 7/ Address 8 | GPMC0_AD7 |
| 66 | P21 | GPMC0_AD6 | GPIO0_21 | 3.3V | GPMC Data 6/ Address 7 | GPMC0_AD6 |
| 68 | P22 | GPMC0_AD5 | GPIO0_20 | 3.3V | GPMC Data 5/ Address 6 | GPMC0_AD5 |
| 70 | P24 | GPMC0_AD4 | GPIO0_19 | 3.3V | GPMC Data 4/ Address 5 | GPMC0_AD4 |
| 72 | N25 | GPMC0_AD3 | GPIO0_18 | 3.3V | GPMC Data 3/ Address 4 | GPMC0_AD3 |
| 74 | N24 | GPMC0_AD2 | GPIO0_17 | 3.3V | GPMC Data 2/ Address 3 | GPMC0_AD2 |
| 76 | N23 | GPMC0_AD1 | GPIO0_16 | 3.3V | GPMC Data 1/ Address 2 | GPMC0_AD1 |
| 78 | M25 | GPMC0_AD0 | GPIO0_15 | 3.3V | GPMC Data 0/ Address 1 | GPMC0_AD0 |
| 80 | - | GND | - | - | Ground | GND |

**Table 7 RIGHT_DOWN (P4) (odd)**

| Num | Ball | Signal | GPIO | Vol | Spec. | Default function |
|---|---|---|---|---|---|---|
| 1 | - | GND | - | - | Ground | GND |
| 3 | F23 | OSPI0_CSN0 | GPIO0_11 | 1.8 | OSPI Chip Select 0 | OSPI0_CSN0 |
| 5 | G21 | OSPI0_CSN1 | GPIO0_12 | 1.8 | OSPI Chip Select 1 | GPIO0_12 |
| 7 | H21 | OSPI0_CSN2 | GPIO0_13 | 1.8 | OSPI Chip Select 2 | OSPI0_CSN2 |
| 9 | E24 | OSPI0_CSN3 | GPIO0_14 | 1.8 | OSPI Chip Select 3 | OSPI0_CSN3 |
| 11 | - | GND | - | - | Ground | GND |
| 13 | E25 | OSPI_DQ0 | GPIO0_3 | 1.8 | OSPI data 0 | OSPI_DQ0 |
| 15 | G24 | OSPI_DQ1 | GPIO0_4 | 1.8 | OSPI data 1 | OSPI_DQ1 |
| 17 | F25 | OSPI_DQ2 | GPIO0_5 | 1.8 V | OSPI data 2 | OSPI_DQ2 |
| 19 | F24 | OSPI_DQ3 | GPIO0_6 | 1.8 | OSPI data 3 | OSPI_DQ3 |
| 21 | - | GND | - | - | Ground | GND |
| 23 | J23 | OSPI_DQ4 | GPIO0_7 | 1.8 | OSPI data 4 | GPIO0_7 |
| 25 | J25 | OSPI_DQ5 | GPIO0_8 | 1.8 | OSPI data 5 | GPIO0_8 |
| 27 | H25 | OSPI_DQ6 | GPIO0_9 | 1.8 | OSPI data 6 | GPIO0_9 |
| 29 | J22 | OSPI_DQ7 | GPIO0_10 | 1.8 | OSPI data 7 | GPIO0_10 |
| 31 | - | GND | - | - | Ground | GND |
| 33 | G25 | OSPI0_LBCL | GPIO0_1 | 1.8 | OSPI loopback clock input | OSPI0_LBCLK |
| 35 | - | GND | - | - | Ground | GND |
| 37 | J24 | OSPI_DQS | GPIO0_2 | 1.8 | OSPI data strobe or | OSPI_DQS |
| 39 | - | GND | - | - | Ground | GND |
| 41 | H24 | OSPI_CLK | GPIO0_0 | 1.8 | OSPI clock output | OSPI_CLK |
| 43 | - | GND | - | - | Ground | GND |
| 45 | U23 | GPMC0_WAIT | GPIO0_37 | 3.3 | GPMC external wait | GPMC0_WAIT0 |
| 47 | V25 | GPIO0_38 | GPIO0_38 | 3.3 | Main domain GPIO0_38 | GPIO0_38 |
| 49 | - | GND | - | - | Ground | GND |
| 51 | M21 | GPMC0_CSN0 | GPIO0_41 | 3.3 | GPMC chip select 0 | GPMC0_CSN0 |
| 53 | L21 | GPIO0_42 | GPIO0_42 | 3.3 | Main domain GPIO0_42 | GPIO0_42 |
| 55 | K22 | GPMC0_CSN2 | GPIO0_43 | 3.3 | GPMC Chip Select 2 | GPMC0_CSN2 |
| 57 | K24 | GPMC0_CSN3 | GPIO0_44 | 3.3 | GPMC Chip Select 3 | GPMC0_CSN3 |
| 59 | - | GND | - | - | Ground | GND |
| 61 | K25 | GPMC0_WPN | GPIO0_39 | 3.3 | GPMC Flash write | GPIO0_39 |
| 63 | L25 | GPMC0_WEN | GPIO0_34 | 3.3 | GPMC write enable | GPMC0_WEN |
| 65 | L24 | GPMC0_OEN | GPIO0_33 | 3.3 | GPMC output enable or | GPMC0_OEN_REN |
| 67 | L23 | | GPIO0_32 | 3.3 | GPMC address valid | |
| 69 | M24 | | GPIO0_35 | 3.3 | GPMC low byte enable or | |
| 71 | M22 | GPMC0_DIR | GPIO0_35 | 3.3 | GPMC data bus signal | GPIO0_40 |
| 73 | N20 | GPMC0_BE1N | GPIO0_36 | 3.3 | GPMC high byte enable | GPIO0_36 |
| 75 | - | GND | - | - | Ground | GND |
| 77 | P25 | GPMC0_CLK | GPIO0_31 | 3.3 | GPMC clock output | GPIO0_31 |
| 79 | - | GND | - | - | Ground | GND |

**Table 8 RIGHT_DOWN (P4 ) (even)**

| Num | Ball | Signal | GPIO | V | Spec. | Default function |
|---|---|---|---|---|---|---|
| 2 | - | GND | - | - | Ground | GND |
| 4 | C21 | MMC1 DATA2 | GPIO1 | 1.8 | MMC1 Data 2 | MMC1 DATA2 |
| 6 | D22 | MMC1 DATA3 | GPIO1 | 1.8 | MMC1 data 3 | MMC1 DATA3 |
| 8 | A21 | MMC1 CMD | GPIO1 | 1.8 | MMC1 command | MMC1 CMD |
| 10 | D17 | MMC1 SDCD | GPIO1 | 3.3 | MMC1 card detection | MMC1 SDCD |
| 12 | - | GND | - | - | Ground | GND |
| 14 | B22 | MMC1 CLK | GPIO1 | 1.8 | MMC1 clock | MMC1 CLK |
| 16 | A22 | MMC1 DATA0 | GPIO1 | 1.8 | MMC1 data 0 | MMC1 DATA0 |
| 18 | B21 | MMC1 DATA1 | GPIO1 | 1.8 | MMC1 Data 1 | MMC1 DATA1 |
| 20 | C17 | GPIO1 49 | GPIO1 | 3.3 | main domain GPIO1 49 | GPIO1 49 |
| twent | - | GND | - | - | Ground | GND |
| twent | E23 | MMC2 DATA2 | GPIO0 | 1.8 | MMC2 Data 2 | MMC2 DATA2 |
| 26 | D24 | MMC2 DATA3 | GPIO0 | 1.8 | MMC2 Data 3 | MMC2 DATA3 |
| 28 | C24 | MMC2 CMD | GPIO0 | 1.8 | MMC2 command | MMC2 CMD |
| 30 | D25 | MMC2 CLK | GPIO0 | 1.8 | MMC2 clock | MMC2 CLK |
| 32 | - | GND | - | - | Ground | GND |
| 34 | B24 | MMC2 DATA0 | GPIO0 | 1.8 | MMC2 data 0 | MMC2 DATA0 |
| 36 | C25 | MMC2 DATA1 | GPIO0 | 1.8 | MMC2 data 1 | MMC2 DATA1 |
| 38 | A23 | GPIO0 71 | GPIO0 | 1.8 | main domain GPIO0 71 | GPIO0 71 |
| 40 | B23 | GPIO0 72 | GPIO0 | 1.8 | main domain GPIO0 72 | GPIO0 72 |
| 42 | - | GND | - | - | Ground | GND |
| 44 | - | VPP 1V8 EN | - | 3.3 | SoM VPP 1V8 enable | VPP 1V8 EN |
| 46 | - | GND | - | - | Ground | GND |
| 48 | - | EXTINTN | - | 3.3 | External interrupt input | EXTINTN |
| 50 | - | RESET REQZ | - | 3.3 | main domain external | RESET REQZ |
| 52 | - | PORZ OUT | - | 3.3 | main domain POR status | PORZ OUT |
| 54 | - | RESETSTATZ | - | 3.3 | main domain warm reset | RESETSTATZ |
| 56 | - | GND | - | - | Ground | GND |
| | | | | | Dual function PMIC | |
| 60 | - | | - | 3.3 | SoM VCC 3V3 Power | |
| 62 | - | GND | - | - | Ground | GND |
| 64 | - | GND | - | - | Ground | GND |
| 66 | - | GND | - | - | Ground | GND |
| 68 | - | GND | - | - | Ground | GND |
| 70 | - | GND | - | - | Ground | GND |
| 72 | - | DCDC 5V | - | 5V | SoM 5V power input | DCDC 5V |
| 74 | - | DCDC_5V | - | 5V | SoM 5V power input | DCDC 5V |
| 76 | - | DCDC 5V | - | 5V | SoM 5V power input | DCDC 5V |
| 78 | - | DCDC 5V | - | 5V | SoM 5V power input | DCDC 5V |
| 80 | - | DCDC 5V | - | 5V | SoM 5V power input | DCDC 5V |

## 2.6 SoM Pin Spec.

### 2.6.1 Power Pin

| Pin | Signal | I/ O | Default function | Pin NO. |
|---|---|---|---|---|
| Power | DCDC_5V | Power input | Som power supplying pin, 5V | P4_72 |
| | DCDC_5V | Power input | Som power supplying pin, 5V | P4_74 |
| | DCDC_5V | Power input | Som power supplying pin, 5V | P4_76 |
| | DCDC_5V | Power input | Som power supplying pin, 5V | P4_78 |
| | DCDC_5V | Power input | Som power supplying pin, 5V | P4_80 |
| | GND | --- | | P1_1 |
| | GND | --- | | P1_2 |
| | GND | --- | | P1_7 |
| | GND | --- | | P1_8 |
| | GND | --- | | P1_13 |
| | GND | --- | | P1_14 |
| | GND | --- | | P1_19 |
| | GND | --- | | P1_20 |
| | GND | --- | | P1_25 |
| | GND | --- | | P1_26 |
| | GND | --- | | P1_31 |
| | GND | --- | | P1_32 |
| | GND | --- | | P1_34 |
| | GND | --- | | P1_36 |
| | GND | --- | | P1_37 |
| | GND | --- | | P1_38 |
| | GND | --- | | P1_40 |
| | GND | --- | | P1_42 |
| | GND | --- | | P1_43 |
| | GND | --- | | P1_44 |
| | GND | --- | | P1_46 |
| | GND | --- | | P1_48 |
| | GND | --- | | P1_49 |
| | GND | --- | | P1_50 |
| | GND | --- | | P1_52 |
| | GND | --- | | P1_54 |
| | GND | --- | | P1_56 |
| | GND | --- | | P1_58 |
| | GND | --- | | P1_60 |
| | GND | --- | | P1_61 |
| | GND | --- | | P1_62 |
| | GND | --- | | P1_63 |
| | GND | --- | | P1_64 |

| GND | --- | | P1_66 |
|---|---|---|---|
| GND | --- | | P1_68 |
| GND | --- | | P1_69 |
| GND | --- | | P1_71 |
| GND | --- | | P1_72 |
| GND | --- | | P1_74 |
| GND | --- | | P1_77 |
| GND | --- | | P1_78 |
| GND | --- | | P1_79 |
| GND | --- | | P1_80 |
| GND | --- | | P2_1 |
| GND | --- | | P2_2 |
| GND | --- | | P2_7 |
| GND | --- | | P2_8 |
| GND | --- | | P2_17 |
| GND | --- | | P2_18 |
| GND | --- | | P2_27 |
| GND | --- | | P2_30 |
| GND | --- | | P2_31 |
| GND | --- | | P2_41 |
| GND | --- | | P2_42 |
| GND | --- | | P2_47 |
| GND | --- | | P2_48 |
| GND | --- | | P2_61 |
| GND | --- | | P2_62 |
| GND | --- | | P2_71 |
| GND | --- | | P2_75 |
| GND | --- | | P2_80 |
| GND | --- | | P2_79 |
| GND | --- | | P2_80 |
| GND | --- | | P3_1 |
| GND | --- | | P3_2 |
| GND | --- | | P3_6 |
| GND | --- | | P3_8 |
| GND | --- | | P3_9 |
| GND | --- | | P3_15 |
| GND | --- | | P3_21 |
| GND | --- | | P3_26 |
| GND | --- | | P3_31 |
| GND | --- | | P3_37 |
| GND | --- | | P3_44 |
| GND | --- | | P3_47 |
| GND | --- | | P3_53 |

| | | | | | |
|---|---|---|---|---|---|
| GND | --- | | | | P3_62 |
| GND | --- | | | | P3_63 |
| GND | --- | | | | P3_69 |
| GND | --- | | | | P3_79 |
| GND | --- | | | | P3_80 |
| GND | --- | | | | P4_1 |
| GND | --- | | | | P4_2 |
| GND | --- | | | | P4_11 |
| GND | --- | | | | P4_12 |
| GND | --- | | | | P4_21 |
| GND | --- | | | | P4_22 |
| GND | --- | | | | P4_31 |
| GND | --- | | | | P4_32 |
| GND | --- | | | | P4_35 |
| GND | --- | | | | P4_39 |
| GND | --- | | | | P4_42 |
| GND | --- | | | | P4_43 |
| GND | --- | | | | P4_46 |
| GND | --- | | | | P4_49 |
| GND | --- | | | | P4_56 |
| GND | --- | | | | P4_59 |
| GND | --- | | | | P4_62 |
| GND | --- | | | | P4_64 |
| GND | --- | | | | P4_66 |
| GND | --- | | | | P4_68 |
| GND | --- | | | | P4_70 |
| GND | --- | | | | P4_75 |
| GND | --- | | | | P4_79 |

## 2.6.2 Boot Pin

| Pin | Signal | I/O | Default function | Pin NO. |
|---|---|---|---|---|
| BOOTMODE | BOOTMODE00 | I | Boot mode 0 | P3_78 |
| | BOOTMODE01 | I | Boot mode 1 | P3_76 |
| | BOOTMODE02 | I | Boot mode 2 | P3_74 |
| | BOOTMODE03 | I | Boot mode 3 | P3_72 |
| | BOOTMODE04 | I | Boot mode 4 | P3_70 |
| | BOOTMODE05 | I | Boot mode 5 | P3_68 |
| | BOOTMODE06 | I | Boot mode 6 | P3_66 |
| | BOOTMODE07 | I | Boot mode 7 | P3_64 |
| | BOOTMODE08 | I | Boot mode 8 | P3_60 |
| | BOOTMODE09 | I | Boot mode 9 | P3_58 |
| | BOOTMODE10 | I | Boot mode 10 | P3_56 |
| | BOOTMODE11 | I | Boot mode 11 | P3_54 |

| BOOTMODE12 | I | Boot mode 12 | P3_52 |
|---|---|---|---|
| BOOTMODE13 | I | Boot mode 13 | P3_50 |
| BOOTMODE14 | I | Boot mode 14 | P3_48 |
| BOOTMODE15 | I | Boot mode 15 | P3_46 |

## 2.6.3 LVDS Output Pin

MAIN Domain

| Pin | Signal | I/O | Default function | Pin NO. |
|---|---|---|---|---|
| LVDS | CH1_LVDS_A0P | O | CH1_LVDS data 0+ | P1_3 |
| | CH1_LVDS_A0N | O | CH1_LVDS data 0- | P1_5 |
| | CH1_LVDS_A1P | O | CH1_LVDS data 1+ | P1_9 |
| | CH1_LVDS_A1N | O | CH1_LVDS data 1- | P1_11 |
| | CH1_LVDS_A2P | O | CH1_LVDS data 2+ | P1_15 |
| | CH1_LVDS_A2N | O | CH1_LVDS data 2- | P1_17 |
| | CH1_LVDS_CLKP | O | CH1_LVDS clock+ | P1_21 |
| | CH1_LVDS_CLKN | O | CH1_LVDS clock- | P1_23 |
| | CH1_LVDS_A3P | O | CH1_LVDS data 3+ | P1_27 |
| | CH1_LVDS_A3N | O | CH1_LVDS data 3- | P1_29 |
| | CH2_LVDS_CLKN | O | CH2_LVDS clock- | P1_33 |
| | CH2_LVDS_CLKP | O | CH2_LVDS clock+ | P1_35 |
| | CH2_LVDS_A1N | O | CH2_LVDS data 1- | P1_39 |
| | CH2_LVDS_A1P | O | CH2_LVDS data 1+ | P1_41 |
| | CH2_LVDS_A2N | O | CH2_LVDS data 2- | P1_45 |
| | CH2_LVDS_A2P | O | CH2_LVDS data 2+ | P1_47 |
| | CH2_LVDS_A0P | O | CH2_LVDS data 0+ | P1_51 |
| | CH2_LVDS_A0N | O | CH2_LVDS data 0- | P1_53 |
| | CH2_LVDS_A3P | O | CH2_LVDS data 3+ | P1_57 |
| | CH2_LVDS_A3N | O | CH2_LVDS data 3- | P1_59 |
| Backlight control | EHRPWM1_A | O | EHRPWM1_A | P2_66 |

## 2.6.4 MIPI CSI

MAIN Domain

| Pin | Signal | I/O | Default function | Pin NO. |
|---|---|---|---|---|
| MIPI CSI | CSI0_RXCLKP | I | CSI0 clock + | P1_4 |
| | CSI0_RXCLKN | I | CSI0 clock - | P1_6 |
| | CSI0_RXP3 | I | CSI0 data receiving 3+ | P1_10 |
| | CSI0_RXN3 | I | CSI0 data receiving 3- | P1_12 |
| | CSI0_RXP1 | I | CSI0 data receiving 1+ | P1_16 |
| | CSI0_RXN1 | I | CSI0 data receiving 1- | P1_18 |
| | CSI0_RXP2 | I | CSI0 data receiving 2+ | P1_22 |
| | CSI0_RXN2 | I | CSI0 data receiving 2- | P1_24 |
| | CSI0_RXP0 | I | CSI0 data receiving 0+ | P1_28 |
| | CSI0_RXN0 | I | CSI0 data receiving 0- | P1_30 |

## 2.6.5 USB

MAIN Domain ：

| Peripheral | Signal | I/O | Default function | Pin No. |
|---|---|---|---|---|
| USB0 | USB0_DP | I/O | USB0 data + | P1_65 |
| | USB0_DM | I/O | USB0 data- | P1_67 |
| | USB0_VBUS | I | USB0 VBUS detect | P1_70 |
| | USB0_DRVBUS | O | USB0 VBUS enabled | P1_77 |
| USB1 | USB1_DP | I/O | USB1 data + | P1_73 |
| | USB1_DM | I/O | USB1 data- | P1_75 |
| | USB1_VBUS | I | USB1 VBUS detect | P1_76 |
| | USB1_DRVBUS | O | USB1 VBUS enabled | P1_79 |

## 2.6.6 Ethernet

MAIN Domain: RGMII

| Peripheral | Signal | I/O | Default function | Pin No. |
|---|---|---|---|---|
| RGMII1 | CPSW_RGMII1_RXC | I | RGMII receiving clock | P3_17 |
| | CPSW_RGMII1_RX_CTL | I | RGMII receiving control | P3_19 |
| | CPSW_RGMII1_RD0 | I | RGMII receiving data 0 | P3_23 |
| | CPSW_RGMII1_RD1 | I | RGMII receiving data 1 | P3_25 |
| | CPSW_RGMII1_RD2 | I | RGMII receiving data 2 | P3_27 |
| | CPSW_RGMII1_RD3 | I | RGMII receiving data 3 | P3_29 |
| | CPSW_RGMII1_TXC | O | RGMII sending clock | P3_33 |
| | CPSW_RGMII1_TX_CTL | O | RGMII sending control | P3_35 |
| | CPSW_RGMII1_TD0 | O | RGMII sending data 0 | P3_39 |
| | CPSW_RGMII1_TD1 | O | RGMII sending data 1 | P3_41 |
| | CPSW_RGMII1_TD2 | O | RGMII sending data 2 | P3_43 |
| | CPSW_RGMII1_TD3 | O | RGMII sending data 3 | P3_45 |
| RGMII2 | CPSW_RGMII1_RXC | I | RGMII receiving clock | P3_49 |
| | CPSW_RGMII1_RX_CTL | I | RGMII receiving control | P3_51 |
| | CPSW_RGMII1_RD0 | I | RGMII receiving data 0 | P3_55 |
| | CPSW_RGMII1_RD1 | I | RGMII receiving data 1 | P3_57 |
| | CPSW_RGMII1_RD2 | I | RGMII receiving data 2 | P3_59 |
| | CPSW_RGMII1_RD3 | I | RGMII receiving data 3 | P3_61 |
| | CPSW_RGMII1_TXC | O | RGMII sending clock | P3_65 |
| | CPSW_RGMII1_TX_CTL | O | RGMII sending control | P3_67 |
| | CPSW_RGMII1_TD0 | O | RGMII sending data 0 | P3_71 |
| | CPSW_RGMII1_TD1 | O | RGMII sending data 1 | P3_73 |
| | CPSW_RGMII1_TD2 | O | RGMII sending data 2 | P3_75 |
| | CPSW_RGMII1_TD3 | O | RGMII sending data 3 | P3_77 |

MAIN Domain ：RMII

| Peripheral | Signal | I/O | Default function | Pin No. |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| RMII1 | RMII1_CRS_DV | I | RMII carrier sense/ data valid | P3_33 |
| | RMII1_REF_CLK | I | RMII reference clock | P3_17 |
| | RMII1_RX_ER | I | RMII receiving data error | P3_19 |
| | RMII1_TX_EN | O | RMII sending enable | P3_35 |
| | RMII1_RXD0 | I | RMII receiving data 0 | P3_23 |
| | RMII1_RXD1 | I | RMII receiving data 1 | P3_25 |
| | RMII1_TXD0 | O | RMII sending data 0 | P3_39 |
| | RMII1_TXD1 | O | RMII sending data 1 | P3_41 |
| RMII2 | RMII2_CRS_DV | I | RMII carrier sense/ data valid | P3_65 |
| | RMII2_REF_CLK | I | RMII reference clock | P3_51 |
| | RMII2_RX_ER | I | RMII receiving data error | P3_51 |
| | RMII2_TX_EN | O | RMII sending enable | P3_67 |
| | RMII2_RXD0 | I | RMII receiving data 0 | P3_55 |
| | RMII2_RXD1 | I | RMII receiving data 1 | P3_57 |
| | RMII2_TXD0 | O | RMII sending data 0 | P3_71 |
| | RMII2_TXD1 | O | RMII sending data 1 | P3_73 |

## 2.6.7 CPTS

MAIN Domain

| Peripheral | Signal | I/O | Default function | Pin No. |
|---|---|---|---|---|
| CPTS | CP_GEMAC_CPTS0_RFT_CLK | O | CPTS reference clock input | LD_72 |
| | CP_GEMAC_CPTS0_TS_COMP | I | CPTS from CPSW3G0 CPTS timestamp counter compare output | LD_70 |
| UART3 | CP_GEMAC_CPTS0_TS_SYNC | O | CPTS timestamp counter output from CPSW3G0 CPTS | LD_29 |
| | CP_GEMAC_CPTS0_HW1TSPUSH | I | CPTS hardware timestamp post input to time sync router | LD_27 |
| UART4 | CP_GEMAC_CPTS0_HW2TSPUSH | I | CPTS hardware timestamp post input to time sync router | LD_41 |
| | SYNC0_OUT | O | CPTS timestamp of the time-synchronized router generator bit 0 output | LD_39 |
| UART5 | SYNC2_OUT | O | CPTS timestamp of the time-synchronized router generator bit 2 output | LD_21 |
| | SYNC3_OUT | I | CPTS timestamp of the time-synchronized router generator bit 3 output | LD_19 |

## 2.6.8 DSS(Display Subsystem)

MAIN Domain

| Peripheral | Signal | I/O | Default function | Pin No. |
|---|---|---|---|---|
| VOUT | VOUT0_DE | O | Video output enable | P3_7 |
| | VOUT0_EXTPCLKIN | I | Video output external pixel clock input | P4_47 |
| | VOUT0_HSYNC | O | Video output horizotal sync | P3_5 |

| VOUT0_PCLK | O | Video output pixel clock output | P3_4 |
|------------|---|--------------------------------|------|
| VOUT0_VSYNC | O | Video output vertical sync | P3_3 |
| VOUT0_DATA0 | O | Video output data 0 | P3_10 |
| VOUT0_DATA1 | O | Video output data 1 | P3_12 |
| VOUT0_DATA2 | O | Video output data 2 | P3_14 |
| VOUT0_DATA3 | O | Video output data 3 | P3_16 |
| VOUT0_DATA4 | O | Video output data 4 | P3_18 |
| VOUT0_DATA5 | O | Video output data 5 | P3_20 |
| VOUT0_DATA6 | O | Video output data 6 | P3_22 |
| VOUT0_DATA7 | O | Video output data 7 | P3_24 |
| VOUT0_DATA8 | O | Video output data 8 | P3_28 |
| VOUT0_DATA9 | O | Video output data 9 | P3_30 |
| VOUT0_DATA10 | O | Video output data 10 | P3_32 |
| VOUT0_DATA11 | O | Video output data 11 | P3_34 |
| VOUT0_DATA12 | O | Video output data 12 | P3_36 |
| VOUT0_DATA13 | O | Video output data 13 | P3_38 |
| VOUT0_DATA14 | O | Video output data 14 | P3_40 |
| VOUT0_DATA15 | O | Video output data 15 | P3_42 |
| VOUT0_DATA16 | O | Video output data 16 | P3_60 |
| VOUT0_DATA17 | O | Video output data 17 | P3_58 |
| VOUT0_DATA18 | O | Video output data 18 | P3_56 |
| VOUT0_DATA19 | O | Video output data 19 | P3_54 |
| VOUT0_DATA20 | O | Video output data 20 | P3_52 |
| VOUT0_DATA21 | O | Video output data 21 | P3_50 |
| VOUT0_DATA22 | O | Video output data 22 | P3_48 |
| VOUT0_DATA23 | O | Video output data 23 | P3_46 |

## 2.6.9 ECAP

| Peripheral | Signal | I/O | Default function | Pin No. |
|------------|--------|-----|------------------|---------|
| ECAP0 | ECAP0_IN_APWM_OUT | IO | ECAP input or assist PWM output | P2_32 |
| ECAP1 | ECAP1_IN_APWM_OUT | IO | ECAP input or assist PWM output | P2_50, P2_66, P2_70, P4_18, P2_63 |
| ECAP2 | ECAP2_IN_APWM_OUT | IO | ECAP input or assist PWM output | P2_52, P2_68, P4_16, P2_78, P2_65 |

## 2.6.10 Emulation and Debug

MAIN Domain ：

| Peripheral | Signal | I/O | Default function | Pin No. |
|------------|--------|-----|------------------|---------|
|  | TRC_CLK | O | Trace clcok | P3_78 |

| TRC_CTL | O | Trace control | P3_76 |
|---|---|---|---|
| TRC_DATA0 | O | Trace data 0 | P3_74 |
| TRC_DATA1 | O | Trace data 1 | P3_72 |
| TRC_DATA2 | O | Trace data 2 | P3_70 |
| TRC_DATA3 | O | Trace data 3 | P3_68 |
| TRC_DATA4 | O | Trace data 4 | P3_66 |
| TRC_DATA5 | O | Trace data 5 | P3_64 |
| TRC_DATA6 | O | Trace data 6 | P4_77 |
| TRC_DATA7 | O | Trace data 7 | P4_67 |
| TRC_DATA8 | O | Trace data 8 | P4_65 |
| TRC_DATA9 | O | Trace data 9 | P4_63 |
| TRC_DATA10 | O | Trace data 10 | P4_69 |
| TRC_DATA11 | O | Trace data 11 | P4_73 |
| TRC_DATA12 | O | Trace data 12 | P4_45 |
| TRC_DATA13 | O | Trace data 13 | P4_61 |
| TRC_DATA14 | O | Trace data 14 | P4_71 |
| TRC_DATA15 | O | Trace data 15 | P4_51 |
| TRC_DATA16 | O | Trace data 16 | P4_53 |
| TRC_DATA17 | O | Trace data 17 | P4_55 |
| TRC_DATA18 | O | Trace data 18 | P4_57 |
| TRC_DATA19 | O | Trace data 19 | P3_46 |
| TRC_DATA20 | O | Trace data 20 | P3_48 |
| TRC_DATA21 | O | Trace data 21 | P3_50 |
| TRC_DATA22 | O | Trace data 22 | P3_52 |
| TRC_DATA23 | O | Trace data 23 | P3_54 |

**MCU Domain**

| Peripheral | Signal | I/O | Default function | Pin No. |
|---|---|---|---|---|
| JTAG | EMU0 | IO | Emulation control 0 | P2_43 |
| | EMU1 | IO | Emulation control 1 | P2_45 |
| | TCK | I | JTAG test clock input | P2_53 |
| | TDI | I | JTAG test data input | P2_57 |
| | TDO | OZ | JTAG test data output | P2_59 |
| | TMS | I | JTAG test mode selection input | P2_55 |
| | TRSTn | I | JTAG reset | P2_51 |

## 2.6.11 EPWM

MAIN Domain

| Peripheral | Signal | I/O | Default function | Pin No. |
|---|---|---|---|---|
| EPWM | EHRPWM_SOCA | O | EHRPWM start to convert A | P2_50 |
| | EHRPWM_SOCB | O | EHRPWM start to convert B | P2_52 |
| | EHRPWM_TZn_IN0 | I | EHRPWM trigger zone input 0(lower power valid) | P2_40 |
| | EHRPWM_TZn_IN3 | I | EHRPWM trigger zone input 3(lower power valid) | P2_44 |
| | EHRPWM_TZn_IN4 | I | EHRPWM trigger zone input 4(lower power valid) | P2_46 |
| | EHRPWM_TZn_IN5 | I | EHRPWM trigger zone input 5(lower power valid) | P2_32 |
| EPWM0 | EHRPWM0_A | IO | EHRPWM output A | P2_34 P2_74 |
| | EHRPWM0_B | IO | EHRPWM output B | P2_72, P2_32, |
| | EHRPWM0_SYNCI | I | Synchronously input from external pin to EHRPWM | P2_54 |

| | EHRPWM0_SYNCO | O | Synchronously output from external pin to | P2_56 |
|---|---|---|---|---|
| EPWM1 | EHRPWM1_A | IO | EHRPWM output A | P2_38, P2_66 |
| | EHRPWM1_B | IO | EHRPWM output B | P2_36, P2_64 |
| EPWM2 | EHRPWM2_A | IO | EHRPWM output A | P2_54, P2_63 |
| | EHRPWM2_B | IO | EHRPWM output B | P2_56, P2_65, |

## 2.6.12 EQEP

MAIN Domain

| Peripheral | Signal | I/O | Default function | Pin No. |
|---|---|---|---|---|
| EQEP0 | EQEP0_A | I | EQEP quadrature input A | P2_70 |
| | EQEP0_B | I | EQEP quadrature input B | P2_68 |
| | EQEP0_I | IO | EQEP index | P2_64 |
| | EQEP0_S | IO | EQEP latch | P2_66 |
| EQEP1 | EQEP1_A | I | EQEP quadrature input A | P2_78 |
| | EQEP1_B | I | EQEP quadrature input B | P2_76 |
| | EQEP1_I | IO | EQEP index | P2_72 |
| | EQEP1_S | IO | EQEP latch | P2_74 |
| EQEP2 | EQEP2_A | I | EQEP quadrature input A | P3_59, P2_50 |
| | EQEP2_B | I | EQEP quadrature input B | P3_61, P2_52 |
| | EQEP2_I | IO | EQEP index | P3_75, P2_44, P4_47 |
| | EQEP2_S | IO | EQEP latch | P3_77, P2_46, P4_71 |

## 2.6.13 GPMC

Main domain

| Pin | Signal | I/ O | Default function | Pin NO. |
|---|---|---|---|---|
| GPMC | GPMC0_ADVn_ALE | O | GPMC address valid(low power valid) or address latch enable | P4_67 |
| | GPMC0_CLK | O | GPMC clock | P4_77 |
| | GPMC0_DIR | O | GPMC data bus signal direction control | P4_71 |
| | GPMC0_OEn_REn | O | GPMC output enable(low power valid) or read enable(low power valid) | P4_65 |
| | GPMC0_WEn | O | GPMC write enable(low power enable) | P4_63 |
| | GPMC0_WPn | O | GPMC Flash write protection(low power valid) | P4_61 |
| | GPMC0_A0 | OZ | GPMC address 0 output. Only for valid addressing 8-bit data non-multiplexed memory | P3_10 |
| | GPMC0_A1 | OZ | GPMC address 1 output under A/ D | P3_12 |

| | | | | |
|---|---|---|---|---|
| | | | non-multiplexed mode, address 17 output under A/D multiplexed mode | |
| GPMC0_A2 | OZ | GPMC address 2 output under A/ D non-multiplexed mode, address 18 output under A/D multiplexed mode | P3_14 |
| GPMC0_A3 | OZ | GPMC address 3 output under A/ D non-multiplexed mode, address 19 output under A/D multiplexed mode | P3_16 |
| GPMC0_A4 | OZ | GPMC address 4 output under A/ D non-multiplexed mode, address 20 output under A/D multiplexed mode | P3_18 |
| GPMC0_A5 | OZ | GPMC address 5 output under A/ D non-multiplexed mode, address 21 output under A/D multiplexed mode | P3_20 |
| GPMC0_A6 | OZ | GPMC address 6 output under A/ D non-multiplexed mode, address 22 output under A/D multiplexed mode | P3_22 |
| GPMC0_A7 | OZ | GPMC address 7 output under A/ D non-multiplexed mode, address 23 output under A/D multiplexed mode | P3_24 |
| GPMC0_A8 | OZ | GPMC address 8 output under A/ D non-multiplexed mode, address 24 output under A/D multiplexed mode | P3_28 |
| GPMC0_A9 | OZ | GPMC address 9 output under A/ D non-multiplexed mode, address 25 output under A/D multiplexed mode | P3_30 |
| GPMC0_A10 | OZ | GPMC address 10 output under A/ D non-multiplexed mode, address 26 output under A/D multiplexed mode | P3_32 |
| GPMC0_A11 | OZ | GPMC address 11 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P3_34 |
| GPMC0_A12 | OZ | GPMC address 12 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P3_36 |
| GPMC0_A13 | OZ | GPMC address 13 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P3_38 |
| GPMC0_A14 | OZ | GPMC address 14 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P3_40 |
| GPMC0_A15 | OZ | GPMC address 15 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P3_42 |

| GPMC0_A16 | OZ | GPMC address 16 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P3_5 |
|---|---|---|---|
| GPMC0_A17 | OZ | GPMC address 17 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P3_7 |
| GPMC0_A18 | OZ | GPMC address 18 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P3_3 |
| GPMC0_A19 | OZ | GPMC address 19 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P3_4 |
| GPMC0_A20 | OZ | GPMC address 20 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P4_57 |
| GPMC0_A21 | OZ | GPMC address 21 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P4_47 |
| GPMC0_A22 | OZ | GPMC address 22 output under A/ D non-multiplexed mode, unused in A/ D multiplexed mode | P4_61 |
| GPMC0_AD0 | IO | GPMC data 0 input/ output under A/ D non-multiplexed mode, and extra address 1 output under A/D multiplexed mode | P3_78 |
| GPMC0_AD1 | IO | GPMC data 1 input/ output under A/ D non-multiplexed mode, and extra address 2 output under A/D multiplexed mode | P3_76 |
| GPMC0_AD2 | IO | GPMC data 2 input/ output under A/ D non-multiplexed mode, and extra address 3 output under A/D multiplexed mode | P3_74 |
| GPMC0_AD3 | IO | GPMC data 3 input/ output under A/ D non-multiplexed mode, and extra address 4 output under A/D multiplexed mode | P3_72 |
| GPMC0_AD4 | IO | GPMC data 4 input/ output under A/ D non-multiplexed mode, and extra address 5 output under A/D multiplexed mode | P3_70 |
| GPMC0_AD5 | IO | GPMC data 5 input/ output under A/ D non-multiplexed mode, and extra address 6 output under A/D multiplexed mode | P3_68 |
| GPMC0_AD6 | IO | GPMC data 6 input/ output under A/ D non-multiplexed mode, and extra address 7 output under A/D multiplexed mode | P3_66 |
| GPMC0_AD7 | IO | GPMC data 7 input/ output under A/ D non-multiplexed mode, and extra address 8 output | P3_64 |

| | | | under A/D multiplexed mode | |
|---|---|---|---|---|
| GPMC0_AD8 | IO | GPMC data 8 input/ output under A/ D non-multiplexed mode, and extra address 9 output under A/D multiplexed mode | P3_60 |
| GPMC0_AD9 | IO | GPMC data 9 input/ output under A/ D non-multiplexed mode, and extra address 10 output under A/D multiplexed mode | P3_58 |
| GPMC0_AD10 | IO | GPMC data 10 input/ output under A/ D non-multiplexed mode, and extra address 11 output under A/D multiplexed mode | P3_56 |
| GPMC0_AD11 | IO | GPMC data 11 input/ output under A/ D non-multiplexed mode, and extra address 12 output under A/D multiplexed mode | P3_54 |
| GPMC0_AD12 | IO | GPMC data 12 input/ output under A/ D non-multiplexed mode, and extra address 13 output under A/D multiplexed mode | P3_52 |
| GPMC0_AD13 | IO | GPMC data 13 input/ output under A/ D non-multiplexed mode, and extra address 14 output under A/D multiplexed mode | P3_50 |
| GPMC0_AD14 | IO | GPMC data 14 input/ output under A/ D non-multiplexed mode, and extra address 15 output under A/D multiplexed mode | P3_48 |
| GPMC0_AD15 | IO | GPMC data 15 input/ output under A/ D non-multiplexed mode, and extra address 16 output under A/D multiplexed mode | P3_46 |
| GPMC0_BE0n_CLE | O | GPMC low byte enable(low power valid) or command latch enable | P4_69 |
| GPMC0_BE1n | O | GPMC high byte enable(low power valid) | P4_73 |
| GPMC0_CSn0 | O | GPMC chip select 0 | P4_51 |
| GPMC0_CSn1 | O | GPMC chip select 1 | P4_53 |
| GPMC0_CSn2 | O | GPMC chip select 2 | P4_55 |
| GPMC0_CSn3 | O | GPMC chip select 3 | P4_57 |
| GPMC0_WAIT0 | I | GPMC external wait indication | P4_45 |
| GPMC0_WAIT1 | I | GPMC external wait indication | P4_47 |

## 2.6.14 IIC

MAIN Domain

| Peripheral | Signal | I/O | Default function | Pin No. |
|---|---|---|---|---|
| IIC0 | I2C0_SCL | IOD | IIC clock | P2_50 |
| | I2C0_SDA | IOD | IIC data | P2_52 |
| IIC1 | I2C1_SCL | IOD | IIC clock | P2_54 |
| | I2C1_SDA | IOD | IIC data | P2_56 |
| IIC2 | I2C2_SCL | IOD | IIC clock | P4_55 |
| | I2C2_SDA | IOD | IIC data | P4_57 |

| IIC3 | I2C3_SCL | IOD | IIC clock | P2_67 |
|------|----------|-----|-----------|-------|
|      | I2C3_SDA | IOD | IIC data  | P2_69 |

MAIN Domain

| Peripheral | Signal | I/O | Default function | Pin No. |
|------------|--------|-----|------------------|---------|
| MCU_I2C0 | MCU_I2C0_SCL | IOD | IIC clock | P2_19 |
|          | MCU_I2C0_SDA | IOD | IIC data  | P2_21 |

WKUP Domain

| Peripheral | Signal | I/O | Default function | Pin No. |
|------------|--------|-----|------------------|---------|
| WKUP_I2C0 | WKUP_I2C0_SCL | IOD | IIC clock | P2_23 |
|           | WKUP_I2C0_SDA | IOD | IIC data  | P2_25 |

## 2.6.15 MCAN

Main Domain

| Peripheral | Signal | I/O | Pin No. |
|------------|--------|-----|---------|
| MCAN0 | MCAN0_RX | I | P2_46 |
|       | MCAN0_TX | O | P2_44 |

MCU Domain

| Peripheral | Signal | I/O | Pin No. |
|------------|--------|-----|---------|
| MCU_MCAN0 | MCU_MCAN0_RX | I | P2_4 |
|           | MCU_MCAN0_TX | O | P2_6 |
| MCU_MCAN1 | MCU_MCAN1_RX | I | P2_3 |
|           | MCU_MCAN1_TX | O | P2_5 |

## 2.7.16 MCASP

MAIN Domain

| Peripheral | Signal | I/O | Pin No. |
|------------|--------|-----|---------|
| MCASP0 | MCASP0_ACLKR | IO | P2_72 |
|        | MCASP0_ACLKX | IO | P2_78 |
|        | MCASP0_AFSR | IO | P2_74 |
|        | MCASP0_AFSX | IO | P2_76 |
|        | MCASP0_AXR0 | IO | P2_64 |
|        | MCASP0_AXR1 | IO | P2_66 |
|        | MCASP0_AXR2 | IO | P2_68 |
|        | MCASP0_AXR3 | IO | P2_70 |
| MCASP1 | MCASP1_ACLKR | IO | P4_30, P4_9, P4_57 |
|        | MCASP1_ACLKX | IO | P4_38, P4_27, P4_69 |
|        | MCASP1_AFSR | IO | P4_28, P4_7, P4_55 |
|        | MCASP1_AFSX | IO | P4_40, P4_29, P4_45 |

| | MCASP1_AXR0 | IO | P4_34, P4_25, P4_63 |
|---|---|---|---|
| | MCASP1_AXR1 | IO | P4_36, P4_23, P4_65 |
| | MCASP1_AXR2 | IO | P4_24, P4_7, P4_67 |
| | MCASP1_AXR3 | IO | P4_26, P4_9, P4_77 |
| | MCASP1_AXR4 | IO | P4_28, P4_55 |
| | MCASP1_AXR5 | IO | P4_30, P4_57 |
| | MCASP2_ACLKR | IO | P3_73, P3_46 |
| | MCASP2_ACLKX | IO | P3_77, P2_69, P3_50 |
| | MCASP2_AFSR | IO | P3_57, P3_48 |
| | MCASP2_AFSX | IO | P2_67, P3_75, P3_52 |
| | MCASP1_AXR0 | IO | P3_59, P2_44, P3_60 |
| MCASP2 | MCASP1_AXR1 | IO | P3_49, P2_46, P3_58 |
| | MCASP1_AXR2 | IO | P3_55, P3_56 |
| | MCASP1_AXR3 | IO | P3_51, P3_54 |
| | MCASP1_AXR4 | IO | P3_67, P3_78 |
| | MCASP1_AXR5 | IO | P3_65, P3_76 |
| | MCASP1_AXR6 | IO | P3_74, P3_71 |
| | MCASP1_AXR7 | IO | P3_57, P3_72 |
| | MCASP1_AXR8 | IO | P3_73, P3_70 |

| | MCASP1_AXR9 | IO | | P3_68 |
|---|---|---|---|---|
| | MCASP1_AXR10 | IO | | P3_66 |
| | MCASP1_AXR11 | IO | | P3_64 |
| | MCASP1_AXR12 | IO | | P4_73 |
| | MCASP1_AXR13 | IO | | P4_71 |
| | MCASP1_AXR14 | IO | | P4_51 |
| | MCASP1_AXR15 | IO | | P4_53 |

## 2.7.17 MCSPI

**MAIN Domain：**

| Function | Signal name | I/O | Default function | PIN number |
|---|---|---|---|---|
| MCSPI0 | SPI0_CLK | IO | SPI clock | P2_38 |
| | SPI0_CS0 | IO | SPI chip select 0 | P2_34 |
| | SPI0_CS1 | IO | SPI Chip Select 1 | P2_32 |
| | SPI0_CS2 | IO | SPI Chip Select 2 | P2_67 |
| | SPI0_CS3 | IO | SPI Chip Select 3 | P2_69 |
| | SPI0_D0 | IO | SPI data 0 | P2_36 |
| | SPI0_D1 | IO | SPI data 1 | P2_40 |
| MCSP1 | SPI1_CLK | IO | SPI clock | P4_25 |
| | SPI1_CS0 | IO | SPI chip select 0 | P4_23 |
| | SPI1_CS1 | IO | SPI Chip Select 1 | P4_7 |
| | SPI1_D0 | IO | SPI data 0 | P4_27 |
| | SPI1_D1 | IO | SPI data 1 | P4_29 |
| MCSP2 | SPI2_CLK | IO | SPI clock | P3_17 P2_72 |
| | SPI2_CS0 | IO | SPI chip select 0 | P2_50P 4_74 |
| | SPI2_CS1 | IO | SPI Chip Select 1 | P2_54 P2_78 |
| | SPI2_CS2 | IO | SPI Chip Select 2 | P2_52P 2_66 |
| | SPI2_CS3 | IO | SPI Chip Select 3 | P2_76 |
| | SPI2_D0 | IO | SPI data 0 | P2_70 P2_63 |
| | SPI2_D1 | IO | SPI data 1 | P2_68 P2_65 |

**MCU Domain :**

| Function | Signal name | I/O | Default function | PIN number |
|---|---|---|---|---|
| MCU_MCSPI0 | MCU_SPI0_CLK | IO | SPI clock | P2_20 |
| | MCU_SPI0_CS0 | IO | SPI chip select 0 | P2_26 |
| | MCU_SPI0_CS1 | IO | SPI Chip Select 1 | P2_28 |
| | MCU_SPI0_CS2 | IO | SPI Chip Select 2 | P2_14 P2_3 |
| | MCU_SPI0_CS3 | IO | SPI Chip Select 3 | P2_6 |
| | MCU_SPI0_D0 | IO | SPI data 0 | P2_22 |
| | MCU_SPI0_D1 | IO | SPI data 1 | P2_24 |
| MCU_MCSPI1 | MCU_SPI1_CLK | IO | SPI clock | P2_12 P2_3 |
| | MCU_SPI1_CS0 | IO | SPI chip select 0 | P2_10 |
| | MCU_SPI1_CS1 | IO | SPI Chip Select 1 | P2_5 |
| | MCU_SPI1_CS2 | IO | SPI Chip Select 2 | P2_16 P2_3 |
| | MCU_SPI1_CS3 | IO | SPI Chip Select 3 | P2_4 |
| | MCU_SPI1_D0 | IO | SPI data 0 | P2_13 |
| | MCU_SPI1_D1 | IO | SPI data 1 | P2_15 |

## 2.7.18 MDIO

Main Domain

| Peripheral | Signal | I/O | Pin No. |
|---|---|---|---|
| MDIO0 | MDIO0_MDC | IO | P3_11 |
| | MDIO0_MDIO | IO | P3_13 |

## 2.7.19 MMC

MAIN Domain

| Function | Signal name | I/O | PIN number |
|---|---|---|---|
| MMC1 | MMC1_CLK | IO | P4_14 |
| | MMC1_CMD | IO | P4_8 |
| | MMC1_SDCD | I | P4_10 |
| | MMC1_SDWP* [1] | I | P4_20 |
| | MMC1_DAT0 | IO | P4_16 |
| | MMC1_DAT1 | IO | P4_16 |
| | MMC1_DAT2 | IO | P4_4 |
| | MMC1_DAT3 | IO | P4_6 |
| | MMC2_CLK | IO | P4_30 |
| | MMC2_CMD | IO | P4_28 |

| MMC2* [2] | MMC2_SDCD | I | P2_67, P4_38, P2_54 |
| | MMC2_SDWP | I | P2_56, P2_69, P4_40 |
| | MMC2_DAT0 | IO | P4_34 |
| | MMC2_DAT1 | IO | P4_36 |
| | MMC2_DAT2 | IO | P4_24 |
| | MMC2_DAT3 | IO | P4_26 |

1. MMC1_SDWP on SoM is for eMMC and it is multiplexed. So this pin on carrier board is suspended.

2. MMC2 pins are all 1.8V.

### 2.7.20 OSPI

MAIN Domain

| Function | Signal name | I/O | PIN number |
|---|---|---|---|
| OSPI | OSPI0_CLK | O | P4_41 |
| | OSPI0_DQS | I | P4_37 |
| | OSPI0_ECC_FAIL | I | P4_9 |
| | OSPI0_LBCLKO | IO | P4_33 |
| | OSPI0_CSn0 | O | P4_3 |
| | OSPI0_CSn1 | O | P4_5 |
| | OSPI0_CSn2 | O | P4_7 |
| | OSPI0_CSn3 | O | P4_9 |
| | OSPI0_D0 | IO | P4_13 |
| | OSPI0_D1 | IO | P4_15 |
| | OSPI0_D2 | IO | P4_17 |
| | OSPI0_D3 | IO | P4_19 |
| | OSPI0_D4 | IO | P4_23 |
| | OSPI0_D5 | IO | P4_25 |
| | OSPI0_D6 | IO | P4_27 |
| | OSPI0_D7 | IO | P4_29 |
| | OSPI0_RESET_OUT0 | O | P4_9 |
| | OSPI0_RESET_OUT1 | O | P4_7 |

### 2.7.21 System Pins

MAIN Domain

| Function | Signal name | I/O | PIN number |
|---|---|---|---|
| System Signal | AUDIO_EXT_REFCLK0 | IO | P2_67 P3_67 P2_64 |

| | AUDIO_EXT_REFCLK1 | IO | P2_69<br>P2_76<br>P4_61 |
|---|---|---|---|
| | CLKOUT0 | O | P2_60 |
| | EXTINTn | I | P4_48 |
| | EXT_REFCLK1 | I | P2_60 |
| | OBSCLK0 | O | P2_50*1<br>P3_56 |
| | PORz_OUT | O | P4_52 |
| | RESETSTATz | O | P4_54 |
| | RESET_REQz | I | P4_50 |
| | SYSCLKOUT0 | O | P2_60 |

*1 The default function of this pin is I2C0 , and multiple devices are mounted on SoM, so it is suspended.

MCU Domain

| Function | Signal name | I/O | PIN number |
|---|---|---|---|
| System Signal | MCU_ERRORn | IO | P2_33 |
| | MCU_EXT_REFCLK0 | I | P2_28<br>P2_5 |
| | MCU_OBSCLK0 | O | P2_28 |
| | MCU_PORz | I | P2_35<br>P2_49 |
| | MCU_RESETSTATz | O | P2_39 |
| | MCU_RESETz | I | P2_37 |
| | MCU_SYSCLKOUT0 | O | P2_28 |

WKUP Domain

| Function | Signal name | I/O | PIN number |
|---|---|---|---|
| System Signal | PMIC_LPM_EN0 | O | P4_58 |
| | WKUP_CLKOUT0 | O | P2_29 |

## 2.7.22 TIMER

MAIN Domain

| Function | Signal name | I/O | PIN number |
|---|---|---|---|
| TIMER | TIMER_IO0 | IO | P2_54, P4_6 |
| | TIMER_IO1 | IO | P2_56, P4_4 |
| | TIMER_IO2 | IO | P4_18, P2_44 |
| | TIMER_IO3 | IO | P4_16, P2_46 |
| | TIMER_IO4 | IO | P4_14 |
| | TIMER_IO5 | IO | P2_52, P4_8 |
| | TIMER_IO6 | IO | P2_67, P4_10 |
| | TIMER_IO7 | IO | P2_69, P4_20 |

MCU Domain

| Function | Signal name | I/O | PIN number |
|---|---|---|---|
| MCU_TIMER | MCU_TIMER_IO0 | IO | P2_13, P2_4 |
| | MCU_TIMER_IO1 | IO | P2_15, P2_28 |
| | MCU_TIMER_IO2 | IO | P2_5 |
| | MCU_TIMER_IO3 | IO | P2_3 |

WKUP Domain

| Function | Signal name | I/O | PIN number |
|---|---|---|---|
| WKUP_TIMER | WKUP_TIMER_IO0 | IO | P2_10, P2_6 |
| | WKUP_TIMER_IO1 | IO | P2_12, P2_26 |

### 2.7.23 UART

MAIN Domain ：

| Function | Signal name | I/O | PIN number |
|---|---|---|---|
| UART0 | UART0_CTSn | I | P2_67 |
| | UART0_RTSn | O | P2_69 |
| | UART0_RXD | I | P2_63 |

| | UART0_TXD | O | P2_65 |
|---|---|---|---|
| UART1 | UART1_CTSn | I | P2_70 |
| | UART1_DCDn | I | P2_50 |
| | UART1_DSRn | I | P2_52 |
| | UART1_DTRn | O | P2_44 |
| | UART1_RIn | I | P2_46 |
| | UART1_RTSn | O | P2_68 |
| | UART1_RXD | I | P2_54, P2_74 |
| | UART1_TXD | O | P2_56, P2_72 |
| UART2 | UART2_CTSn | I | P2_16, P3_4, P3_48 |
| | UART2_RTSn | O | P3_3, P4_18, P3_46 |
| | UART2_RXD | I | P2_67, P4_6, P3_60, P3_10 |
| | UART2_TXD | O | P2_69, P4_4, P3_58, P3_12 |
| UART3 | UART3_CTSn | I | P4_20, P3_7 |
| | UART3_RTSn | O | P3_5, P4_10 |
| | UART3_RXD | I | P4_14, P3_56, P3_14, |
| | UART3_TXD | O | P4_8, P3_54, P3_16 |
| UART4 | UART4_CTSn | I | P3_42 |
| | UART4_RTSn | O | P3_40 |
| | UART4_RXD | I | P4_38, P4_55, P3_52, |
| | UART4_TXD | O | P4_40, |

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| | | | P4_57,<br>P3_50,<br>P3_20 |
|---|---|---|---|
| | UART5_CTSn | I | P3_38,<br>P4_37 |
| | UART5_RTSn | O | P3_36,<br>P3_3 |
| UART5 | UART5_RXD | I | P2_44,<br>P4_26,<br>P4_7,<br>P3_48,<br>P3_22 |
| | UART5_TXD | O | P3_24,<br>P2_46,<br>P4_24,<br>P4_9,<br>P3_46 |
| | UART6_CTSn | I | P3_34,<br>P4_29 |
| | UART6_RTSn | O | P4_27,<br>P3_32 |
| UART6 | UART6_RXD | I | P2_70,<br>P4_10,<br>P4_30,<br>P4_23,<br>P3_28,<br>P4_47 |
| | UART6_TXD | O | P2_68,<br>P4_20,<br>P4_28,<br>P4_25,<br>P4_61,<br>P3_30 |

MCU Domain

| Function | Signal name | I/O | PIN number |
|---|---|---|---|
| MCU_UART0 | MCU_UART0_CTSn | I | P2_13 |
| | MCU_UART0_RTSn | O | P2_15 |
| | MCU_UART0_RXD | I | P2_11 |
| | MCU_UART0_TXD | O | P2_9 |

WKUP Domain

| Function | Signal name | I/O | PIN number |
|----------|-------------|-----|------------|
| WKUP_UART0 | WKUP_UART0_CTSn | I | P2_10 |
| | WKUP_UART0_RTSn | O | P2_12 |
| | WKUP_UART0_RXD | I | P2_14 |
| | WKUP_UART0_TXD | O | P2_16 |

# 2.7 SoM Designing Tips

FET6254-C SoM mounted with power, reset monitoring circuit and storage circuit



About the minimum system schematic please refer to Appendix 4. Generally, except for minimum system,

we kindly suggest users mounting some peripherals such as debug to check booting log output

# Chapter 3 OK6254-C Carrier Board Features

## 3.1 Overview
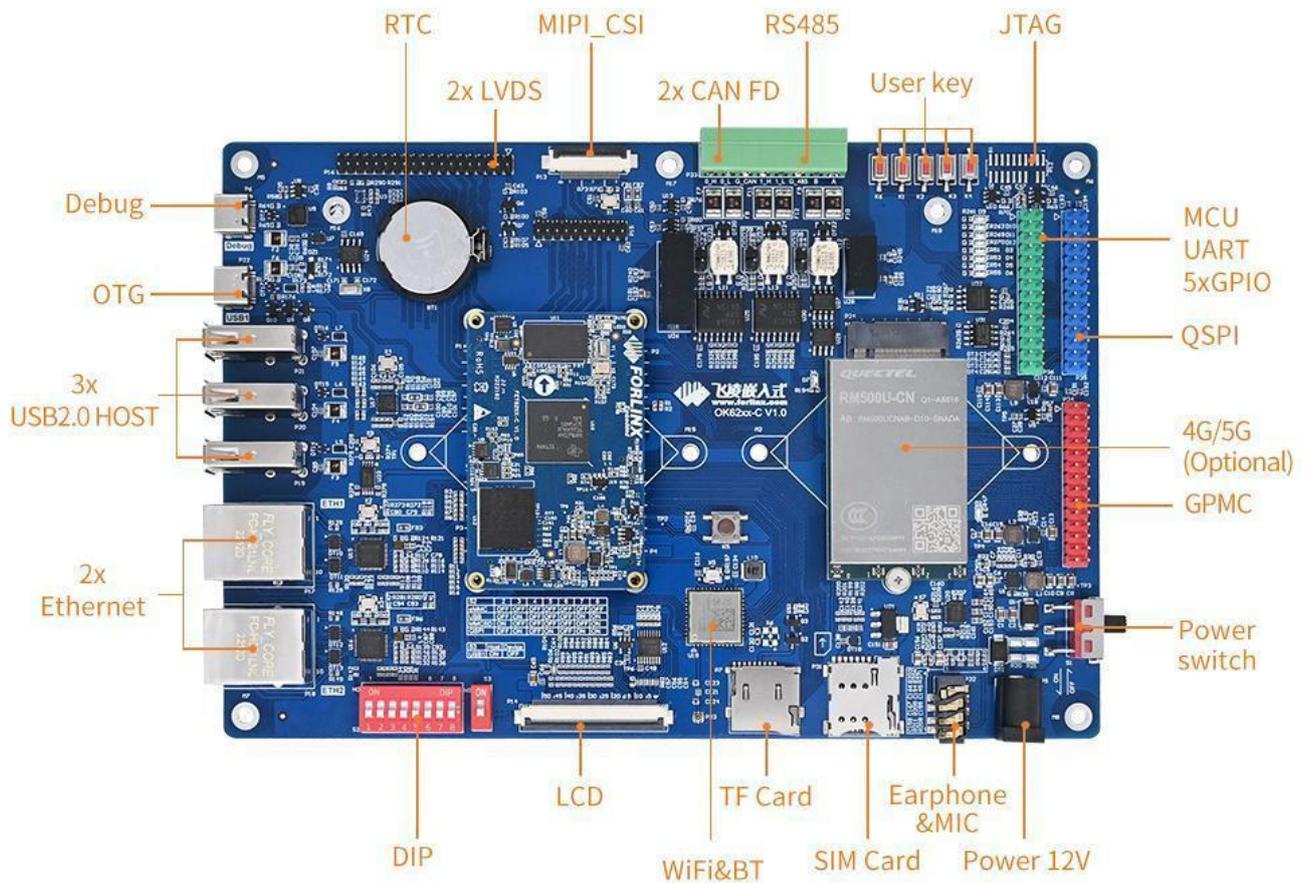
# 3.2 Dimensions
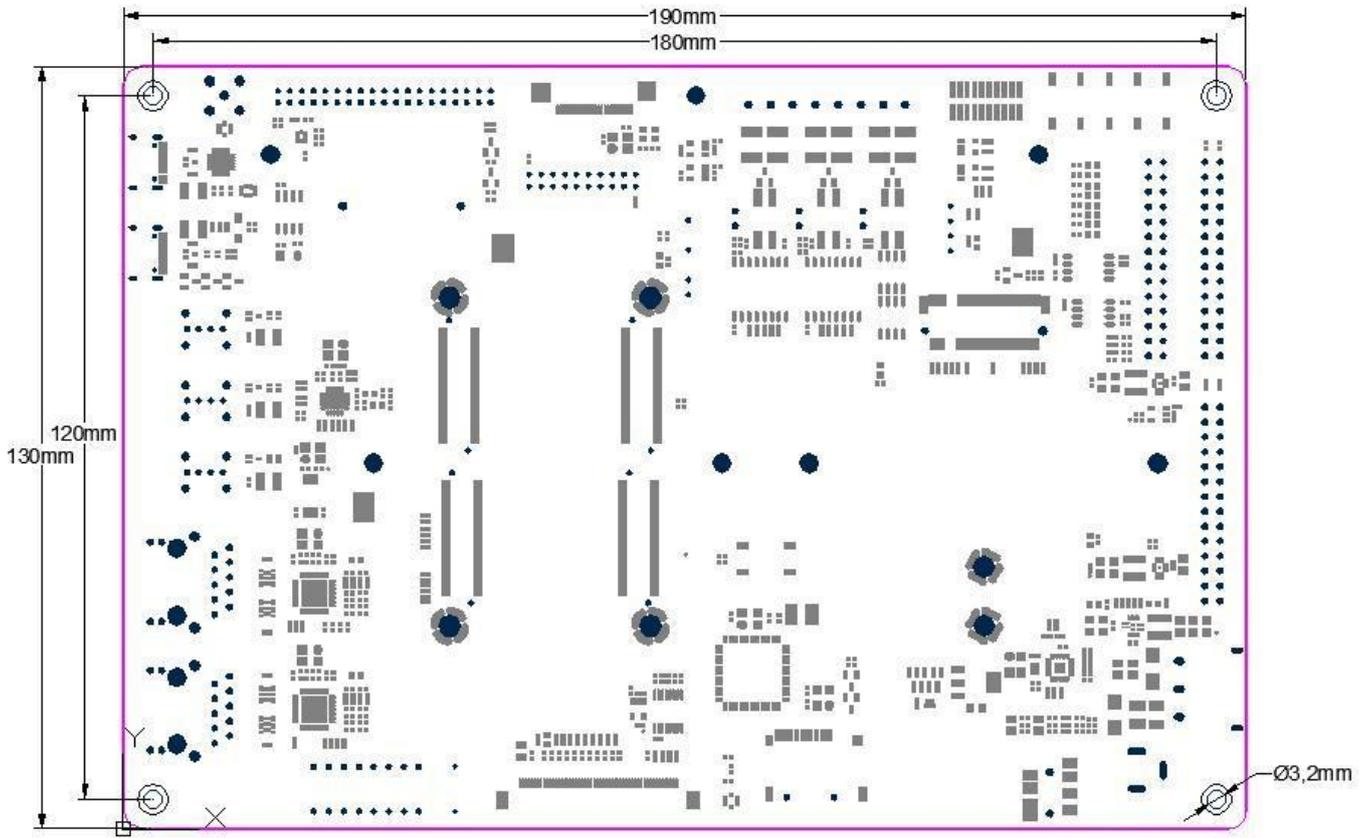


PCB dimensions: 190x 130mm, for more details, please refer to the DXF file;

Mounting hole: pitch: 180mm×120mm, diameter: 3.2mm

PCB processing: thickness 1.6mm, 4-layer

# 3.3 Carrier Board Features

| Peripheral | QTY | Spec. |
|---|---|---|
| LVDS | 2 | Dual asynchronous channels(8 data, 2clocks), supports 1920x1200p60;<br>Available for below three modes:<br>•single LVDS output mode;<br>•2x single LVDS(copy) output mode: two LVDS output same content;<br>•dual LVDS output mode, 8-lane data and 2-lane clock combine to one output channel<br>Default and recommended model: Forlinx 10.1'' LVDS module, 1280x800 @ 60fps |
| RGB parallel | 1 | By FPC connector, 16-bit(RGB565)<br>Default and recommended model: Forlinx 7'' LCD module, 1024x600@ 60fps |
| Camera | 1 | FPC connector<br>Recommended module: OV5645, up to 2592X1944 |
| Ethernet | 2 | 10/100/1000Mbps auto-negotiation, RJ45 |
| USB2.0 | 4 | 3 x USB HOST<br>1 x USB OTG |
| DEBUG UART | 3 | UART0 of A53 and WKUP_UART0 of R5 converted to USB, by Type-C connector |

| | | MCU_UART0 of M4F by 2.54mm pin headers |
|---|---|---|
| RS485 | 1 | Electrical isolated, automatic control of sending and receiving direction<br>Static, surge, group pulse protection level-3 |
| CAN-FD | 2 | Electrical isolated, CAN-FD up to 5Mbps<br>Static, surge, group pulse protection level-3 |
| SPI | 1 | MCU_SPI0 by pin headers with pitch of 2.54mm<br>Rating up to 50 MHz |
| I2C | 2 | MCU_I2C0 and WKUP_I2C0 are by pin headers with pitch of 2.54mm |
| GPMC | 1 | GPMC_AD0~AD15 by pin headers with pitch of 2.54mm, 16-bit data/ address signals and related control signal |
| Audio | 1 | 1x earphone output and 1x MIC input |
| TF-CARD | 1 | 1x TF Card slot, supports UHS-I TF card, up to 104MB/s |
| 4G/5G | 1 | 4G and 5G are optional and alternative;<br>4G: M.2 Key B 4G module, recommended model: Quectel EM05(default), EC20;<br>5G: M.2 Key B 5G module, recommended model: Quectel RM500U-CN;<br>Standard MicroSIM card slot |
| WiFi | 1 | On-boardAW-CM358M;<br>IEEE 802.11 a/b/g/n/ac dual-band WIFI, up to 433.3Mbps; |
| Bluetooth | 1 | Bluetooth 5, up to 3Mbps |
| KEY | 5 | 4 keys input for A53, 1 key input for M4F |
| LED | 8 | 4 LED out put for A53, 4 LED output for M4F |
| RTC | 1 | On-board separate RTC chip |
| EEPROM | 1 | 2K bit<br>Mounted to MCU_I2C0 or WKUP_I2C0 |
| QSPI Flash | 1 | 128M bit<br>Mounted to A53 QSPI or MCU SPI0 |
| JTAG | 1 | By 2 x 10-Pin pin headers with pitch of 1.27mm |

# 3.4 Carrier Board Introduction

Note: components tag with marks of '_DNP' means the components are not soldered.

## 3.5.1 Power

The carrier board is equipped with a DC12V power adapter. S1 on carrier board is the power key, and it is designed with TVS, and over current protection by F1, D1 together with F1 for anti-reverse operation.
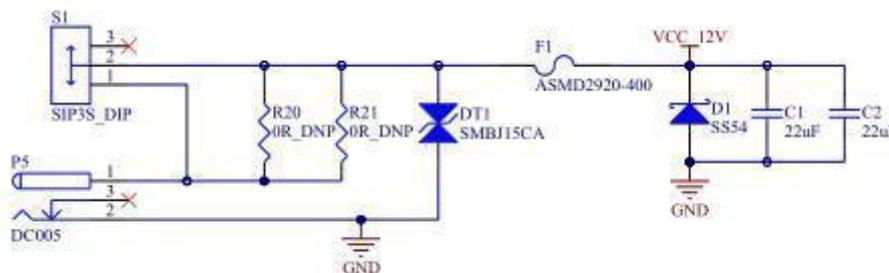
VCC_12V will lowered to VCC_5V through U1, and then supply power to SoM, this ensures the SoM could be powered on first
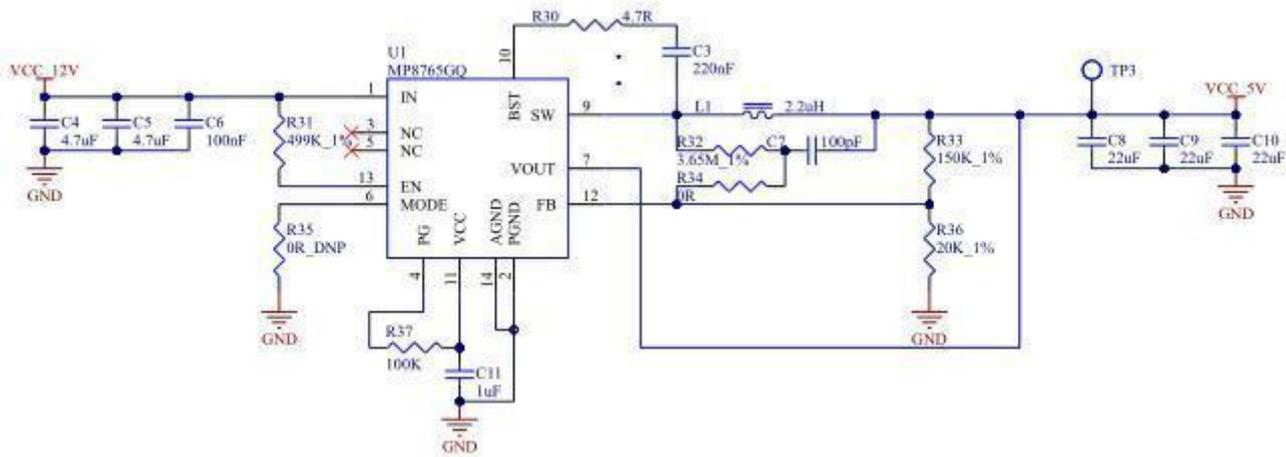


VCC_5V will lowered to VCC_3V3 through U2. U2 is controlled by POWER_EN(it's up-pulled to SoM 3.3V by 100K resistor, and will be released when the SoM critical power is finished). VCC_3V3 supplies power to all 3.3V carrier board devices.
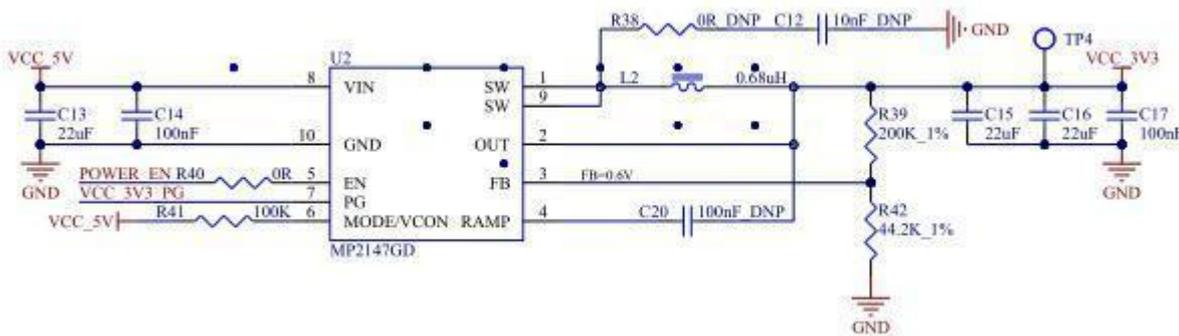


VCC_5V is controlled by U4 to output VDD_5V . U4 is controlled by PG from U2, when VCC_3V3 is to powered, U4 will be turn on. VDD_5V supplies power to part of 5V devices.
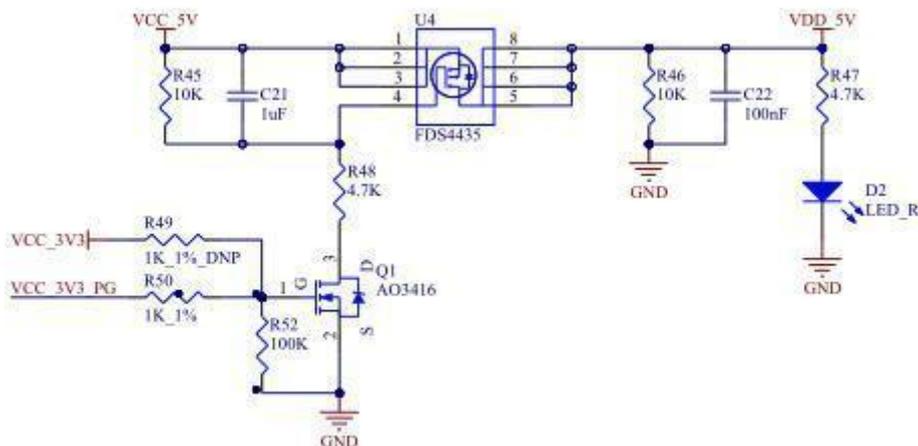


VCC_3V3 will be lowered to VCC_1V8 through U5 and supplier power to carrier board 1.8V.
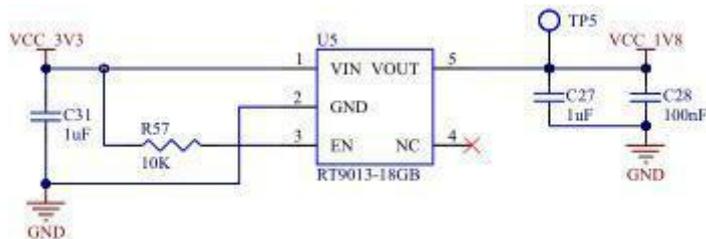
VCC_5V will be lowered to VCC_3V3_TOUCH through U6, and supply power to resitive touching chip.

Please notice that VCC_3V3_TOUCH should powered with SoM at the same time.
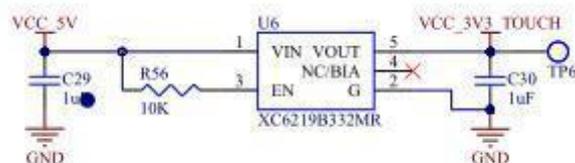


Note:

1. When designing carrier board, please ensure power-on sequence of the power;

We kindly suggest users choose voltage converting chips with perfect power circuit

## 3.5.2 Reset

RESET_REQZ is SoM reset signal input, to make it convenient to debug, it's connected to the key.
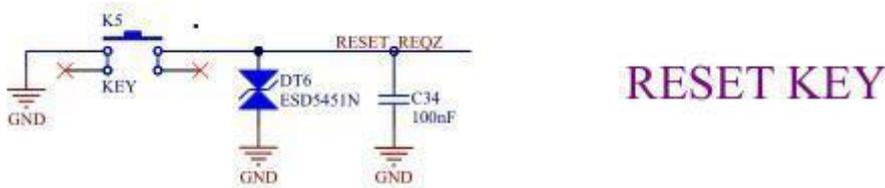


## 3.5.3 Boot Mode

GPMC0_AD0 ~ GPMC0_AD15 on SoM are respectively for BOOTMODE00 ~ BOOTMODE15 .

BOOTMODE Pin Mapping：

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Backup Boot Mode Config | Backup Boot Mode | | | Primary Boot Mode config | | | Primary Boot Mode | | | | PLL Config | | |

BOOTMODE[02:00]: CPU PLL , it's configured to BOOTMODE[02:00] = 011 on SoM, and it's not

needed to be configured on carrier board again;

BOOTMODE[03:06]：request boot(master) mode after POR, that boot from it peripheral/ RAM, it's

configured to BOOTMODE[03:06] = 0001 on SoM;

BOOTMODE[07:09]: it's configured to BOOTMODE[07:09] = 000 on SoM

BOOTMODE[10:12]: backup boot mode option, when the master booting mode fails, then system will

boot from the backup booted peripheral/ memory. It's configured to BOOTMODE[10:12] = 011;

BOOTMODE[13]: backup booting mode optional, works together with the selected booting mode. It's

configured to BOOTMODE[13]：0 on SoM;

BOOTMODE[14:15]: preserved pins, it's configured to BOOTMODE[14:15] = 00 on SoM.

Primary Boot Mode Selection：

| | Primary Boot Mode Config | | | | | | Primary Boot Mode |
|---|---|---|---|---|---|---|---|
| B9 | B8 | B7 | B6 | B5 | B4 | B3 | |
| Reserved | Read Mode2 | Read Mode1 | 0 | 0 | 0 | 0 | Serial NAND |
| Reserved | Iclk | Csel | 0 | 0 | 0 | 1 | OSPI |
| Reserved | Iclk | Csel | 0 | 0 | 1 | 0 | QSPI |
| Reserved | Mode | Csel | 0 | 0 | 1 | 1 | SPI |
| Clkout | 0 | Link Info | 0 | 1 | 0 | 0 | Ethernet RGMII |
| Clkout | Clk src | 0 | 0 | 1 | 0 | 1 | Ethernet RMII |
| Bus reseet | Reserved | Ader | 0 | 1 | 1 | 0 | I2C |
| Reserved | Reserved | Reserved | 0 | 1 | 1 | 1 | UART |
| 1 | Reserved | Fs/raw | 1 | 0 | 0 | 0 | MMCSD Boot(SD Card Boot or eMMC Boot using UDA) |
| Reserved | Reserved | Reserved | 1 | 0 | 0 | 1 | eMMC Boot |
| Core Volt | Mode | Lane Swap | 1 | 0 | 1 | 0 | USB |
| Reserved | Reserved | Reserved | 1 | 0 | 1 | 1 | GPMC NAND |
| Reserved | Reserved | Reserved | 1 | 1 | 0 | 0 | GPMC NOR |
| Reserved | Reserved | Reserved | 1 | 1 | 0 | 1 | Reserved |
| SFPD | Read Cmd | Mode | 1 | 1 | 1 | 0 | Xspi |
| Reserved | ARM/Thumb | No/Dev | 1 | 1 | 1 | 1 | No-boot/Dev boot |

OK6254-C can support multiplex booting modes by DIP S2 on carrier board
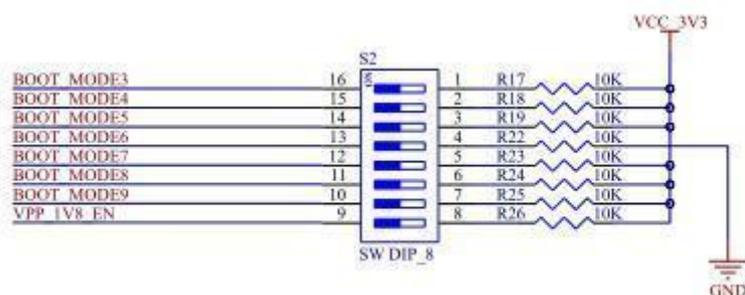


Users can choose booting mode by switching DIP to ON/ OFF, S2 order is the sequence of DIP switch,

S2 is marked with 1~ 8 on PCB, the 8th doesn't matter with booting mode.

| Boot Media | S2 Order | | | | | | |
|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| eMMC | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| TF Card | OFF | OFF | OFF | OFF | OFF | OFF | ON |
| QSPI Flash | ON | ON | OFF | ON | OFF | ON | OFF |
| USB Disk | OFF | ON | OFF | OFF | OFF | ON | OFF |
| USB DFU | OFF | ON | OFF | OFF | OFF | OFF | OFF |

## 3.5.4 Debug Port

U9 on carrier board convert SOC UART0 and WKUP UART0 to USB signal and then circuited to    P6

Type-C for debug purpose. To avoid U9 UART signal reverse perfusion to SoM when SoM is not booted,

which may damage the SoM, Forlinx takes U7 for UART signal buffer.
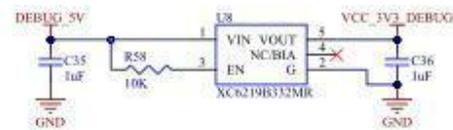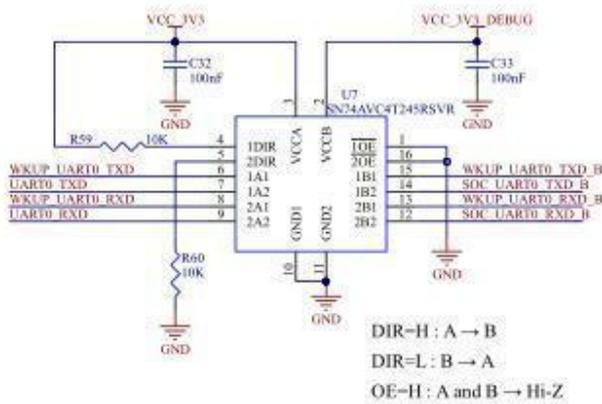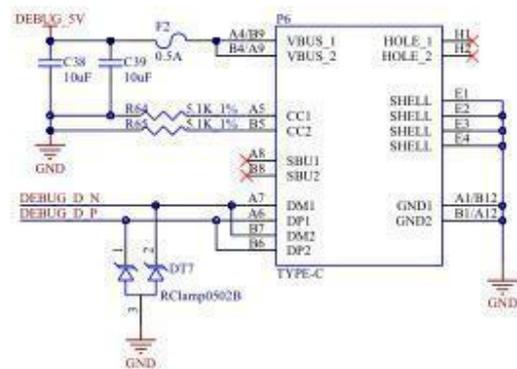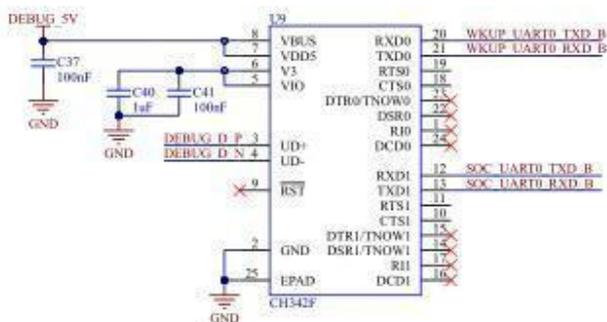


Note:

1. We kindly users have the debug ported designed when designing carrier board, which will be much

convenient and necessary;

2. U7 is just reference circuit, users can take MOS or other solution for current anti-reverse perfusion;

3. U9 is VBUS of Type-C, which ensures PC to load driver, so that the serial output information is

complete.

## 3.5.5 JTAG

JTAG on carrier board is based on standard TI circuit, so users can use TI's emulator directly.
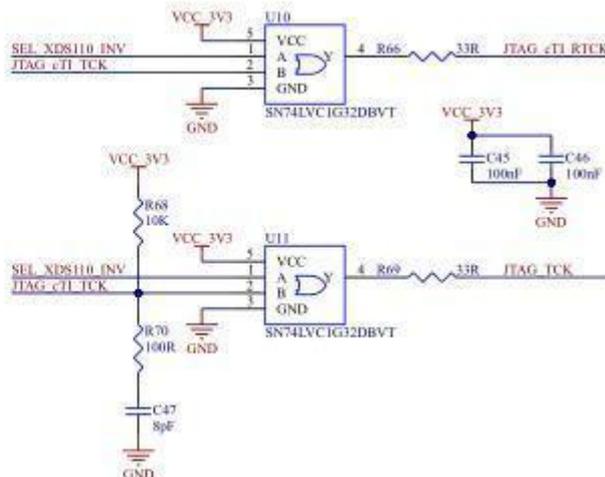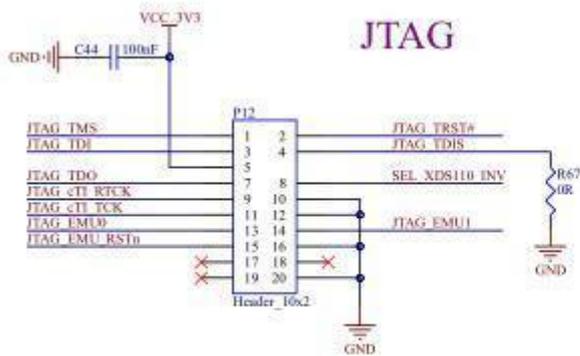
## 3.5.6 LED and User Key

LED and user keys on carrier board consist of main domain and MCU domain.

Main domain integrates LED and user key together. What should be noticed is that when test GPIO output, please don't press the key, otherwise, it will forcibly pull GPIO to low power, here below the image is for Main domain.
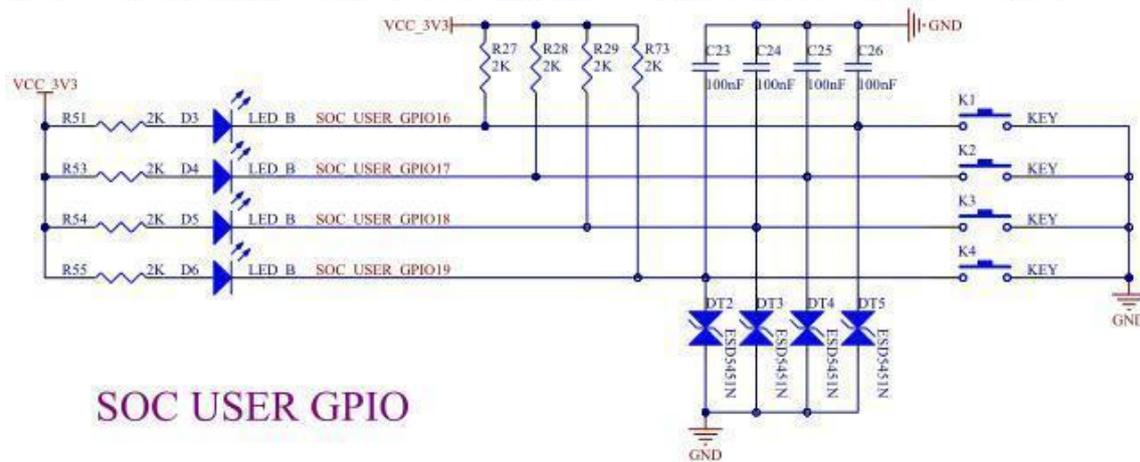


MCU domain has one user key for input and 4 LED as below
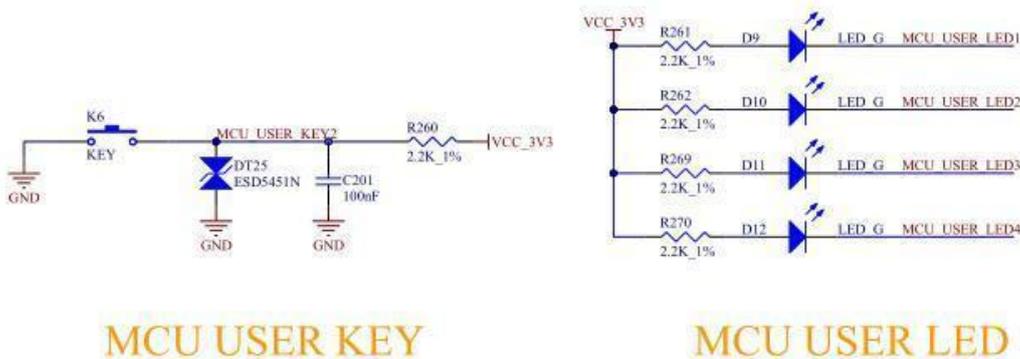
### 3.5.7 Display

FET6254-C SoM can support wo LVDS and one RGB parallel output.

Two LVDS ports are available on P16 by 2x 19P pin headers with pitch of 2.0mm, which can be mounted with Forlinx 10.1'' LVDS display.
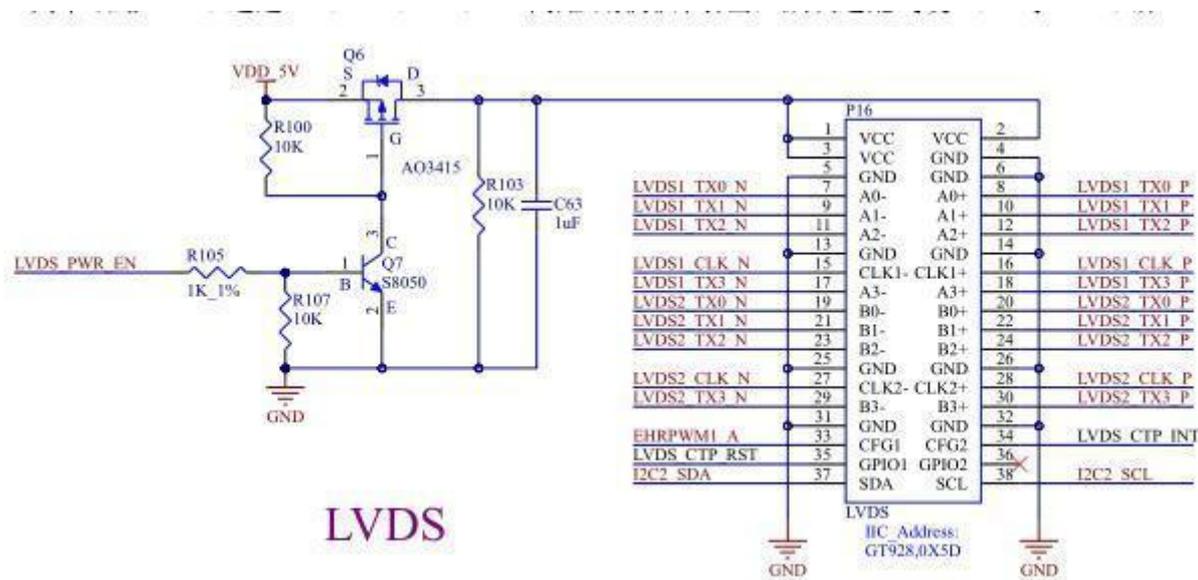


**LVDS**

One RGB parallel port on P14 by a 54-pin FPC cable with pitch of 0.5mm, it can be mounted with Forlinx 7'' LCD module.



**Resistive Touch**
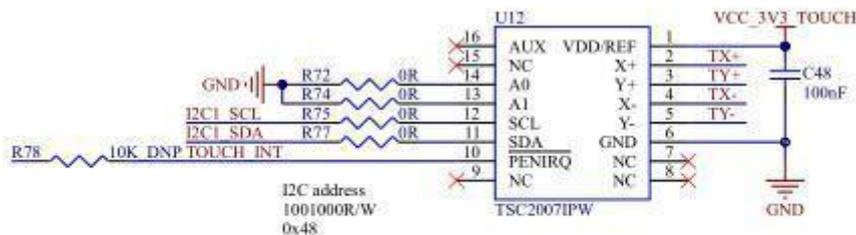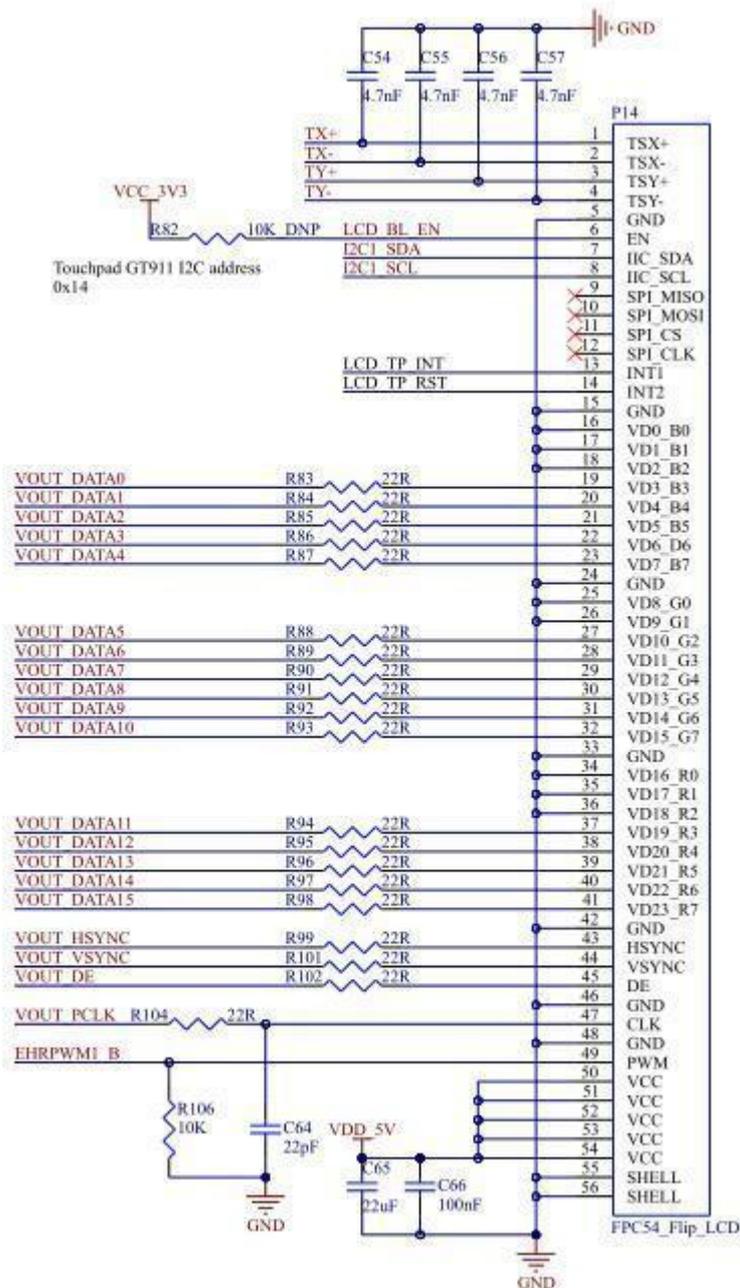
## LCD-RGB565

TP reset and interrupt signals of both 7'' LCD and 10.1'' LVDS display are 3.3V, while the four GPIO of CPU are 1.8V, so power converting is needed, and also the signals are bidirectional.
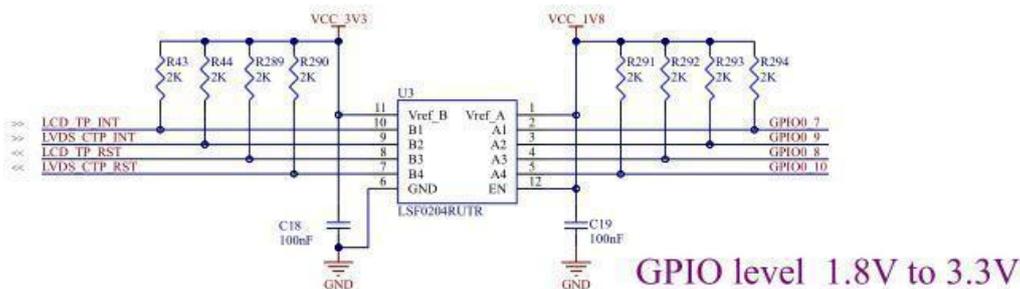


GPIO level  1.8V to 3.3V

Note:

1. Please distribute RGB signals correctly;

2. Please don't mount LCD and LVDS touch chips to the same IIC;

3. Impedance requirement: single end 50oh; differential 100ohm.

## 3.5.8 Video Input

The SoM supports one MIPI DPHY 4Lanes input, it's available on carrier board by P15 2x10P 2.0mm pin headers for 4 Lanes backup. And by P13 26P with pitch of 0.5mm for 2 Lanes FPC for Forlinx OV5645 module.
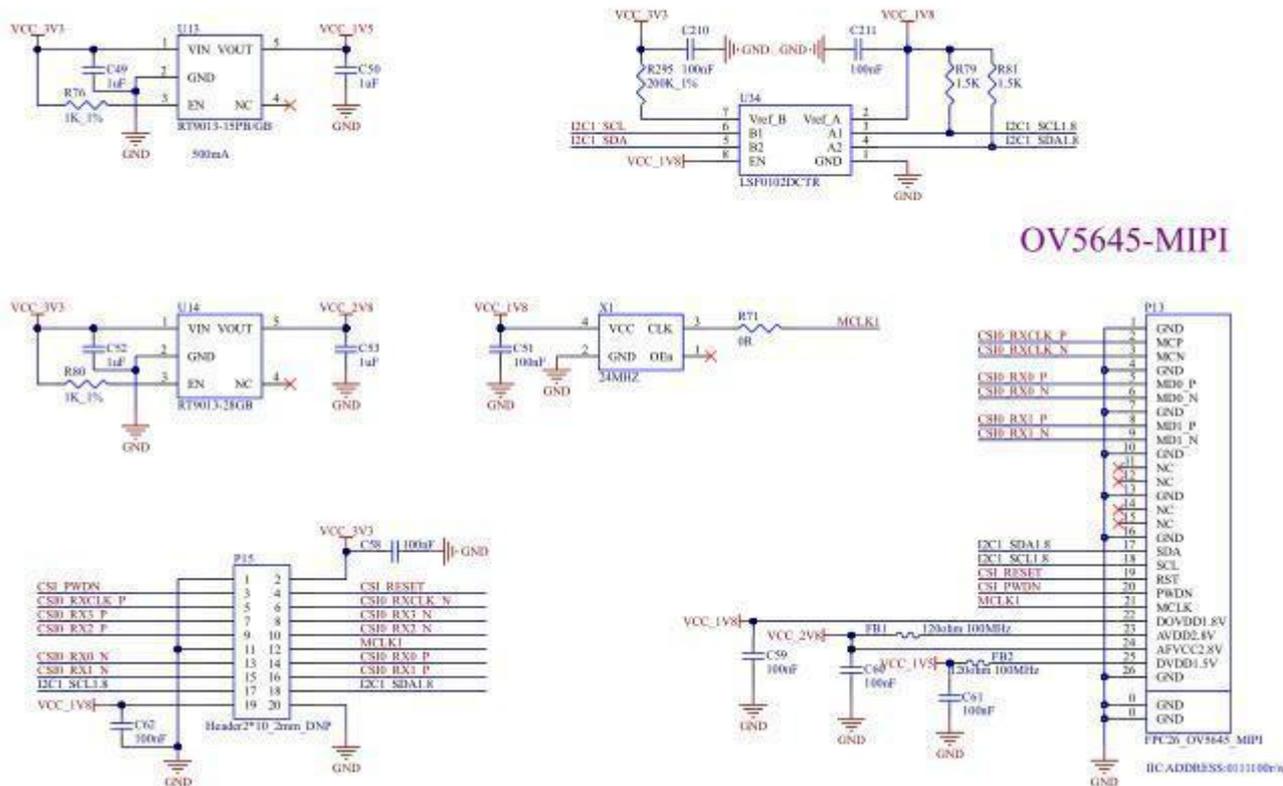


Note:

1. IIC power should be matched properly;

2. Power supply of camera should be with magnetic bead for filter;

3. Impedance requirement: differential 100ohm

## 3.5.9 TF Card

P7 on carrier board is for TF card which could be used for system booting and firmware installing
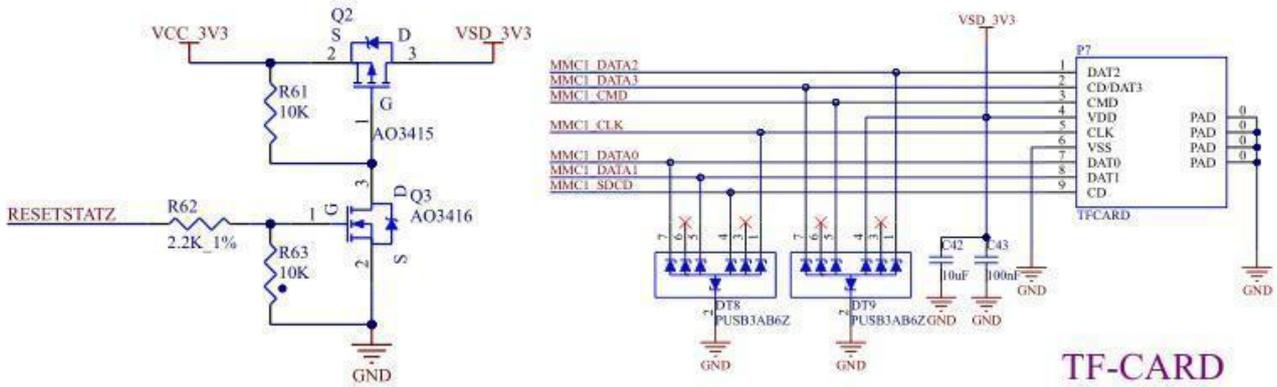
TF-CARD

Note:

1. TF card power supply should be controlled, please refer to Forlinx carrier board circuit;

2. Impedance: single end 50ohm.

## 3.5.10 Ethernet

There are two 10/100/1000M Ethernet ports available on carrier board by RJ45 connectors.

Note:

1. RGMII IO is 3.3V, so it should be the same at the PHY chip end;

2. PCB layout should be with complete RGMII reference plane, and PHY peripheral power with complete reference plane;

3. The two PHY chips are mounted to the same MDC MDIO, please notice that the addresses should not be conflict;

4. Equal length requirement: RGMII receiving end and sending end should be equal length ≤1 1 2.5 mil;

1. Impedance: single end 50ohm

## 3.5.11 USB

SoM can support two USB2.0, USB1 is expanded to three USB2.0 Host by HUB, and the three ports are available on carrier board by P19, P20 and P21.

USB2.0-HUB

USB2.0-HOST

USB0 is configured to OTG and is available as Type-C on carrier board. Host mode and device mode could be controlled by DIP S3, OFF for Device mode and ON for Host mode.



USB2.0-TYPE-C

Note:

1.It needs to add ESD protection to the data line;

2.impedance requirement: differential 90ohm

### 3.5.12 4G/ 5G

P24 M.2 Key-B is for 4G and 5G modems, but please notice that they could not be used together. P31 is for SIM card slot.



M.2 4G&5G
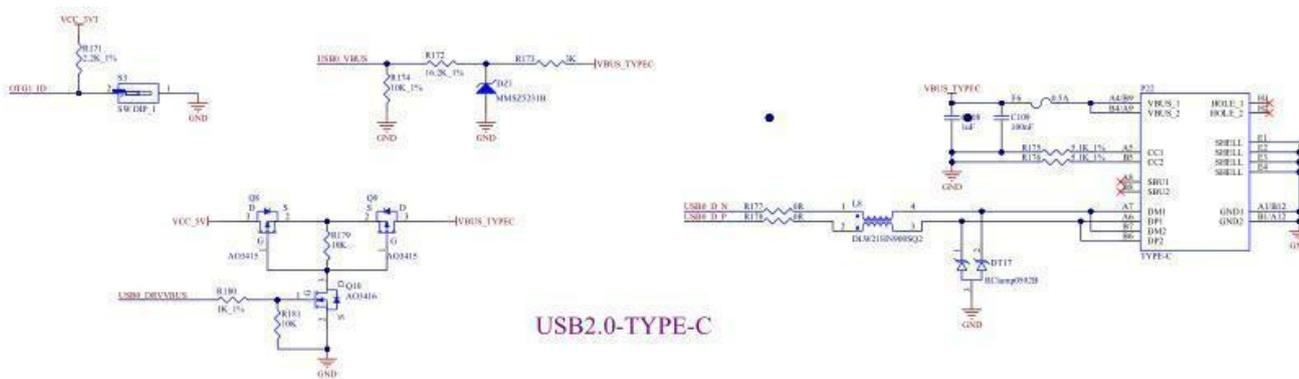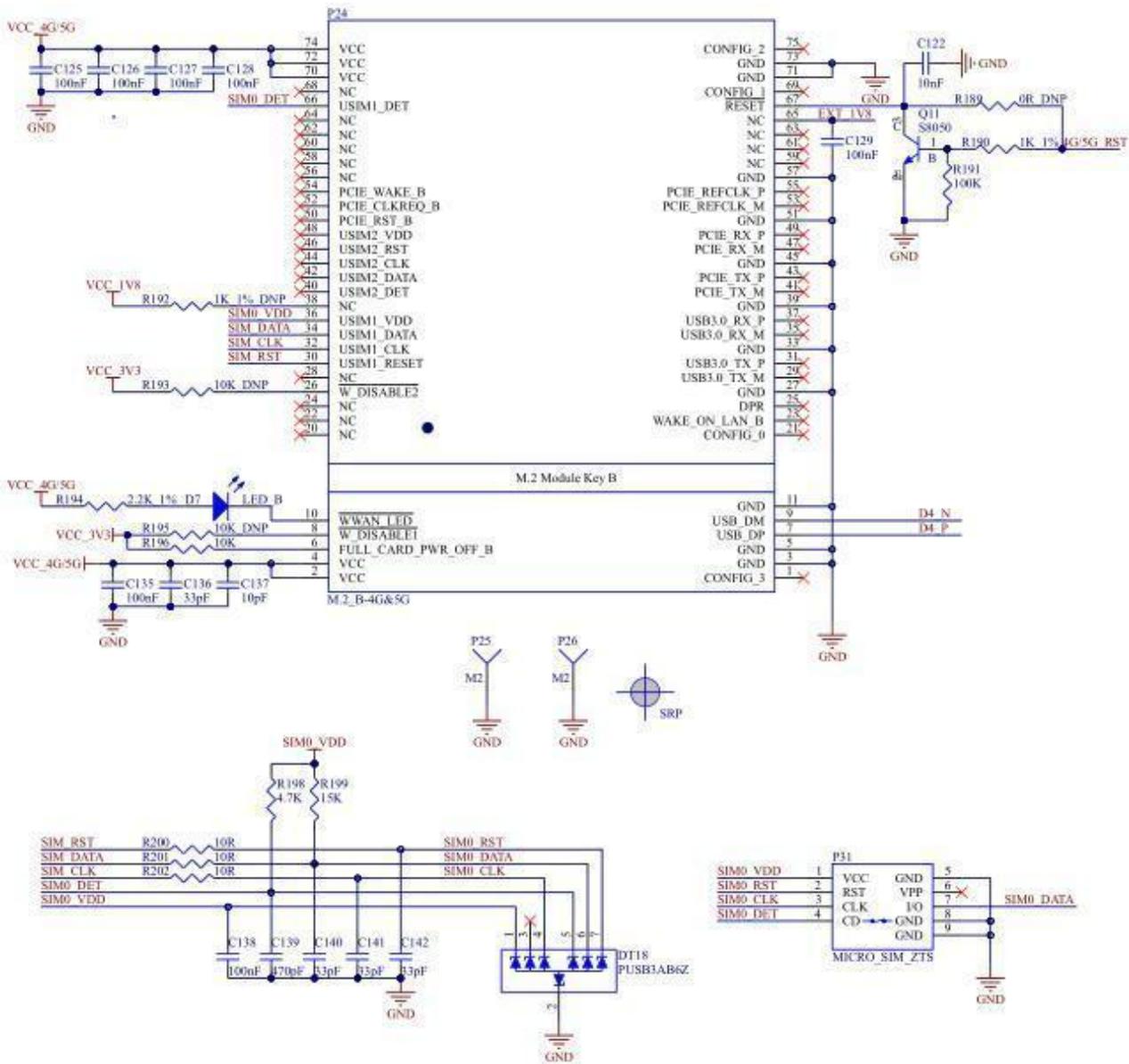
### 3.5.13 WiFi& BT

There is CAM358 WIFI&BT module available on carrier board.
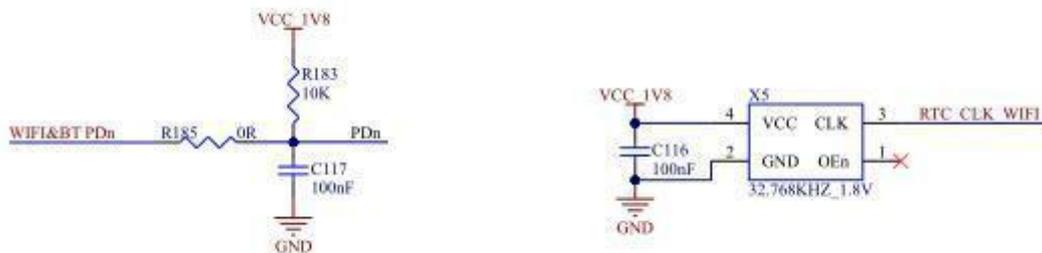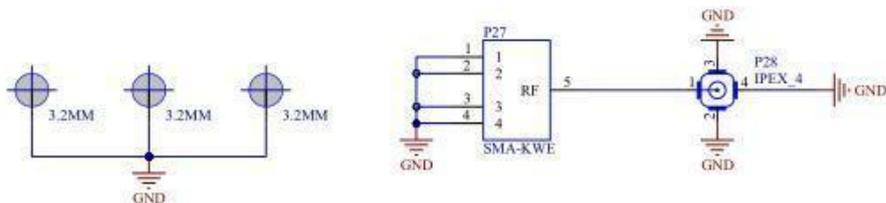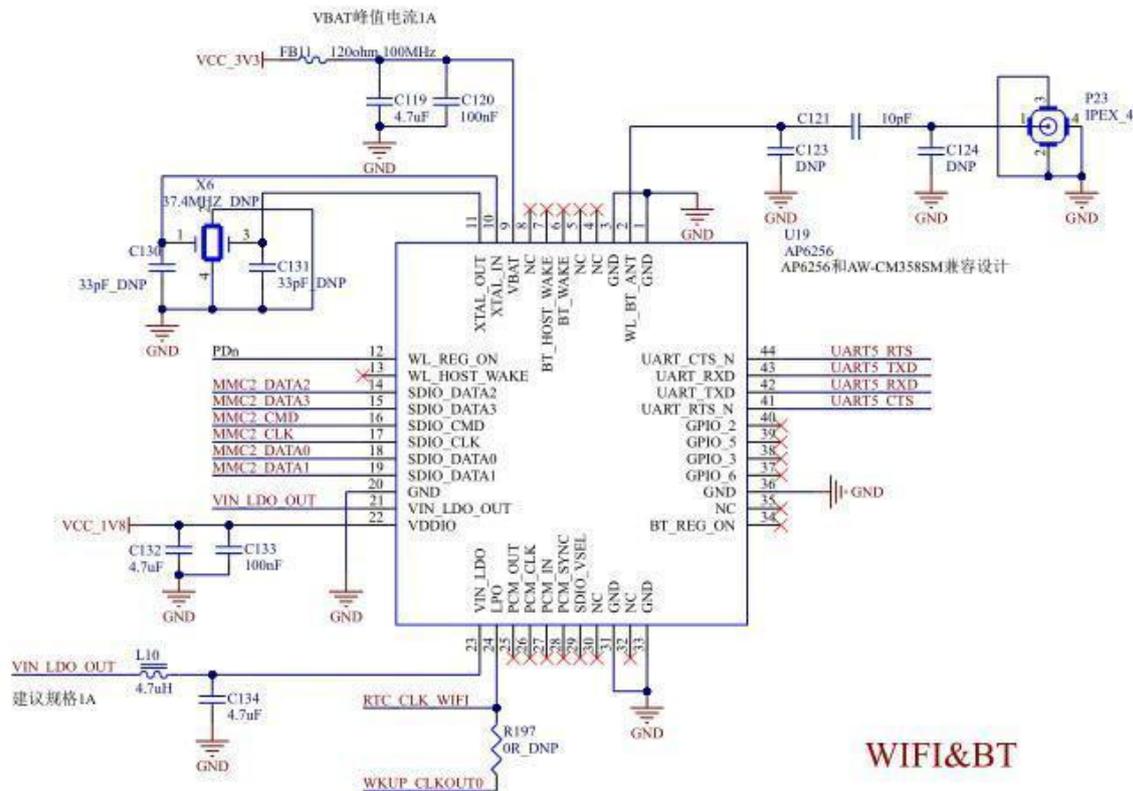
Note:

Impedance: single end 50ohm.

### 3.5.14 Audio

The carrier board is integrated with ES8388 audio codec chip, can support earphone output and MIC input

**AUDIO**

note: analog signal reflow zone and digital signal reflow zone should be separated on PCB layout to avoid serial interference.

## 3.5.15 RTC

Recommended RTC battery model: CR2023



**RTC**

## 3.5.16 QSPI Flash

Main domain and MCU domain which one to be mounted to QSPI Flash could be controlled by jumper wire.
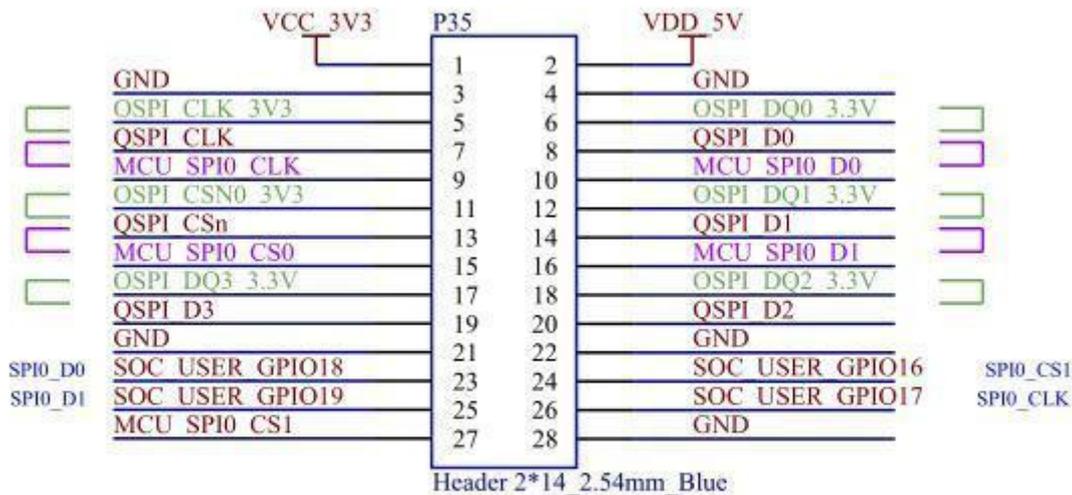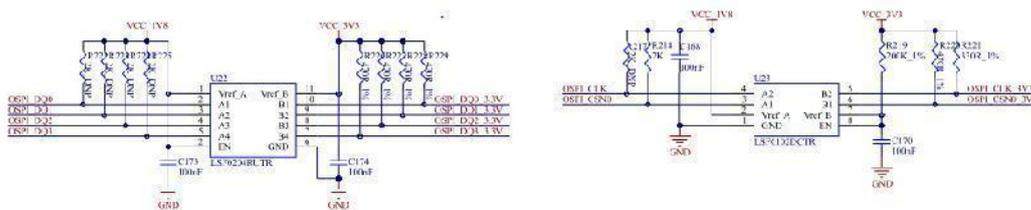
QSPI



QSPI 1.8V to 3.3V
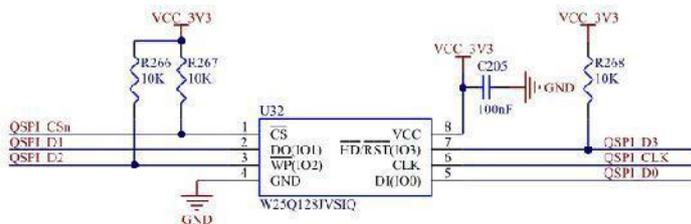


QSPI Flash

### 3.5.17 GPMC

OK3568-C carries WiFi& BT module AW-CM358SM on board, WLAN complies with IEEE 802.11 a/b/g/n/ac dual-band WiFi up to 433.3Mbps, and BT5 up to 3Mbps. To strengthen signal, please use a 2.4G& 5GHz WiFi antenna.

Note: audio function is not available for BT, SD signal should be equal length.

### 3.5.18 PCIe2.1

GPMC is available on carrier board P34 by 2x 14 pin headers with pitch of 2.54mm, can support 16-bit address data multiplexed.
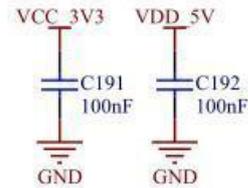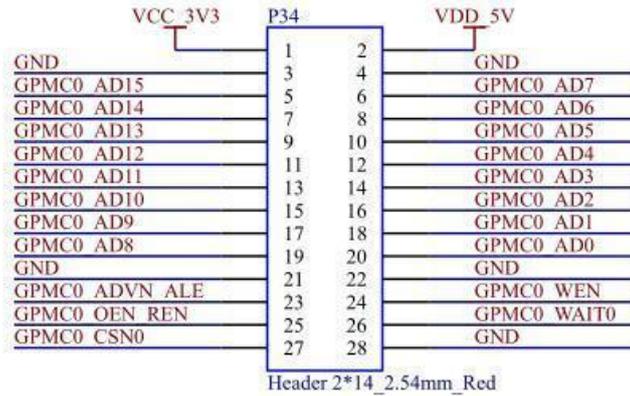
GPMC

## 3.5.18 CAN&RS485

The carrier board has two CAN FD and one RS485 available on it. One CAN FD for Main domain and one for MCU domain.
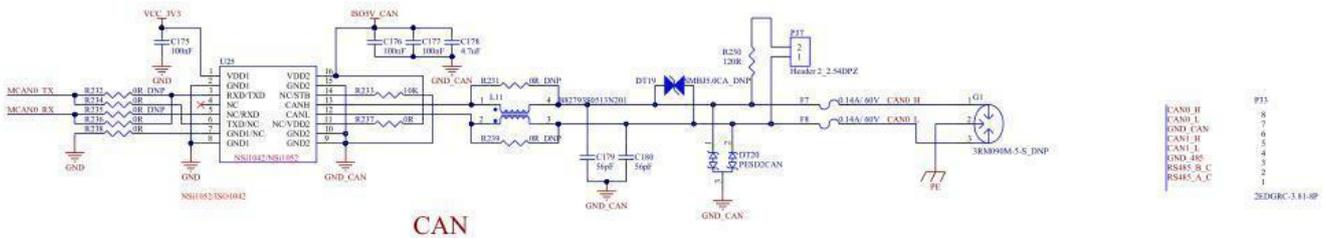


CAN
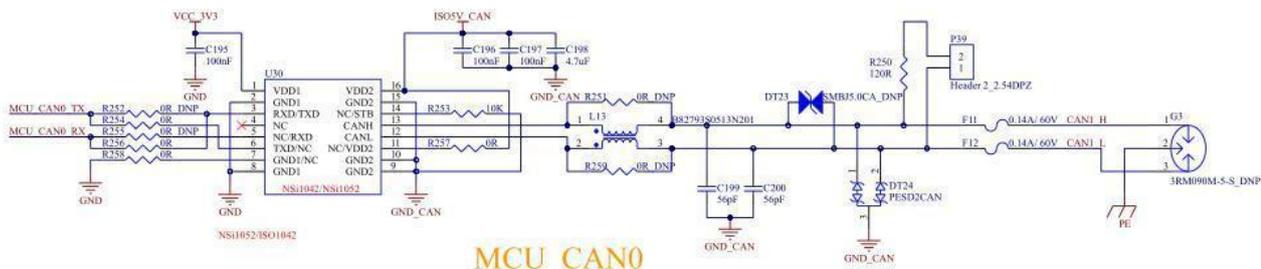


MCU_CAN0
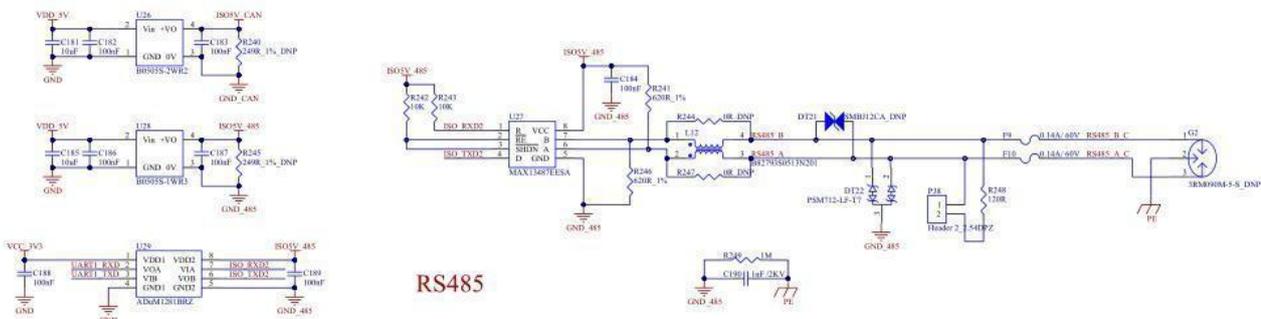


RS485

Note:

1. CAN and RS485 should be with necessary solution for EMC testing, if no EMC testing or just need low level EMC testing, users can do some change according to the real condition;

2. GND isolate part please refer to Forlinx carrier board circuit.

## 3.5.19 EEPROM

MCU domain and WKUP domain which one to be mounted to EEPROM could be controlled by jumper wire.
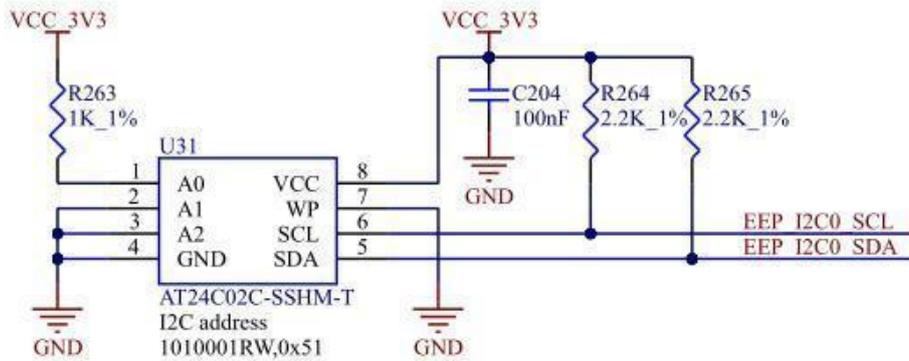


**MCU EEPROM**

## 3.5.20 MCU Pins for Users

MCU pins for users are available on carrier board P36 by 2x 14 pin headers with pitch of 2.54mm.
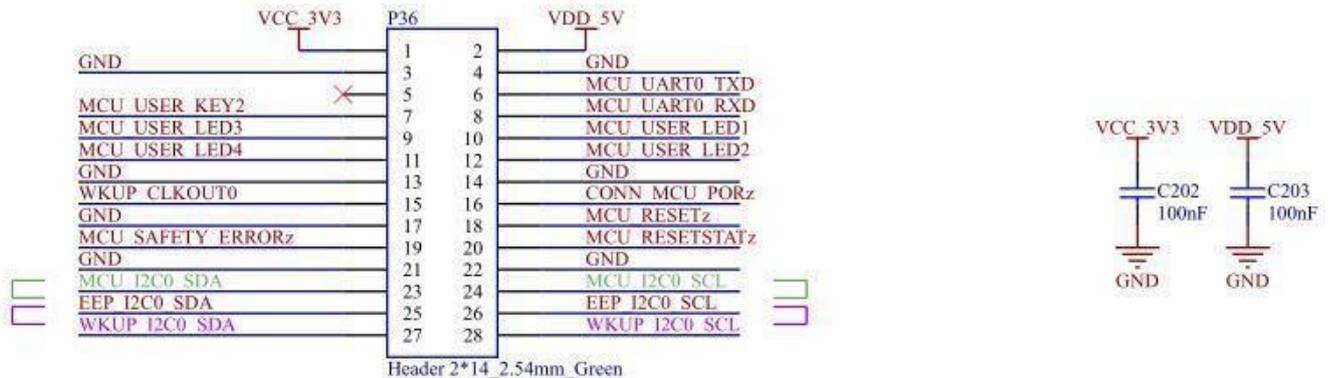


**MCU_USER_IO**

# Appendix

## Appendix 1 Carrier Board Designing Instruction

**Power**

1. when you design carrier board PCB, please make your circuit can ensure the SoM to be powered firstly, and carrier board powering controlled by VCC_3V3_SYS_PG output from SoM;

2. when SoM pins communicates with peripherals directly, please notice problem about current reflow. If the SoM is not powered but peripheral powered firstly, it may cause current reflow to SoM, thus will cause SoM failure. Please control the peripherals to be powered properly or add anti-reflow circuit;

3. some SoM pins are 1.8V, which should be noticed;

4. power supply to TF card should be under control;

5. display interface and USB device power consumption is relative high, please notice specially about the PCB circuit layout and related over-current circuit;

6. PHY chip generally has multiple power supplying pins, such as AVDD, DVDD, DCDD_RGMII and so on, please pay attention to each pin's voltage. Generally, it needs magnetic beads for filtering, and please ensure its around circuit capacitor's value and quantity are enough;

7. we kindly suggest choosing 4.2V power for the 5G cellular module, if the voltage is too low and signal quality is poor, the 5G module maybe disconnected or even restarted;

8. SDIO and UART for WiFi& BT is 1.8V;

9. if isolation is needed for CAN and RS485, both signal and power should be isolated.

**Reset**
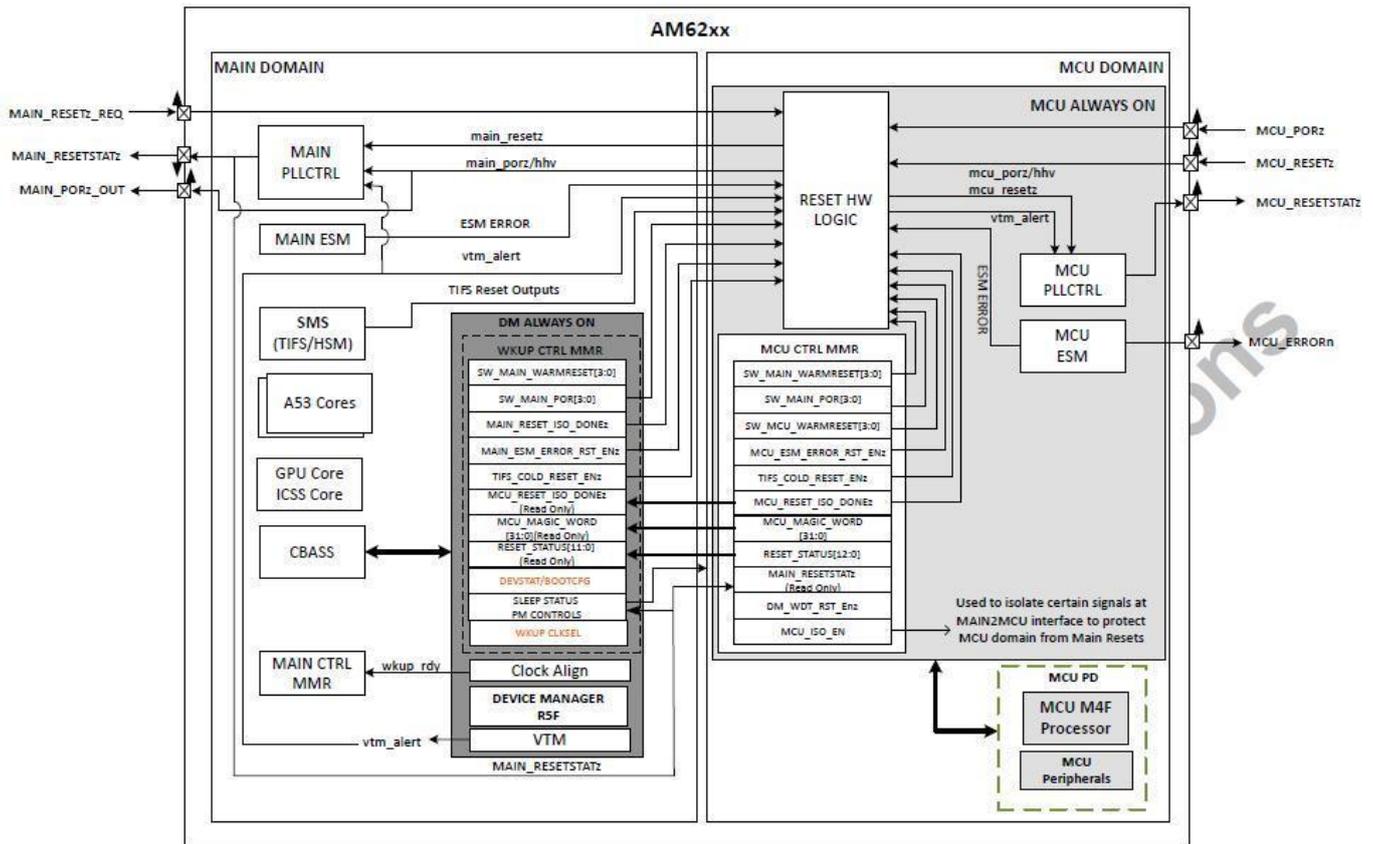
# Appendix 2 Power Consumption

| Hardware | Test item | Supply voltage (V) | Working current (mA) | |
|---|---|---|---|---|
| | | | Instantaneous peak | stable value |
| OK6254-C Evk | Unloaded power-on | 12 | 293 | 234 |
| | Loaded with LVDS+LCD | 12 | 649 | 590 |
| | Loaded with LVDS+LCD+ cpu occupies 90% | 12 | 800 | 770 |
| SoM only | Unloaded power-on | 5 | 552 | 427 |
| | CPU full loaded | 5 | 528 | 480 |

# Appendix 3 Connector Dimensions

Connector model for SoM is AXK6F80337YG

Connector model for carrier board is AXK5F80537YG

| contacts No.\Dimension | A | B | C |
|---|---|---|---|
| 10 | 2.50 | 2.00 | 4.10 |
| 12 | 3.00 | 2.50 | 2.50 |
| 14 | 6.50 | 3.00 | 5.10 |
| 16 | 7.00 | 3.50 | 6.50 |
| 18 | 7.50 | 4.00 | 6.10 |
| 20 | 8.00 | 4.50 | 7.50 |
| 22 | 8.50 | 5.00 | 7.10 |
| 24 | 9.00 | 5.50 | 8.50 |
| 26 | 9.50 | 6.00 | 8.10 |
| 30 | 10.50 | 7.00 | 9.10 |
| 34 | 11.50 | 8.00 | 10.10 |
| 40 | 13.00 | 9.50 | 12.20 |
| 50 | 15.50 | 12.00 | 17.41 |
| 60 | 18.00 | 14.50 | 17.20 |
| 70 | 20.50 | 17.00 | 19.61 |
| 80 | 23.00 | 19.50 | 22.20 |
| 100 | 28.00 | 24.50 | 27.20 |

General tolerance ±0.2

Processes Nickel barrier (Nickel exposure)
Note(1)The vicinity of soldering part

(Top View)

Recommended PC board pattern
(Minimum pad (level))

Settling drawing

AXK6F002○○Y              AXK6F003○○Y
Header used              Header used

Detail "D"
Contact with both-ends chamfered
Mating area

Note

Lot No.

function

# Appendix 4 Minimum System Schematic
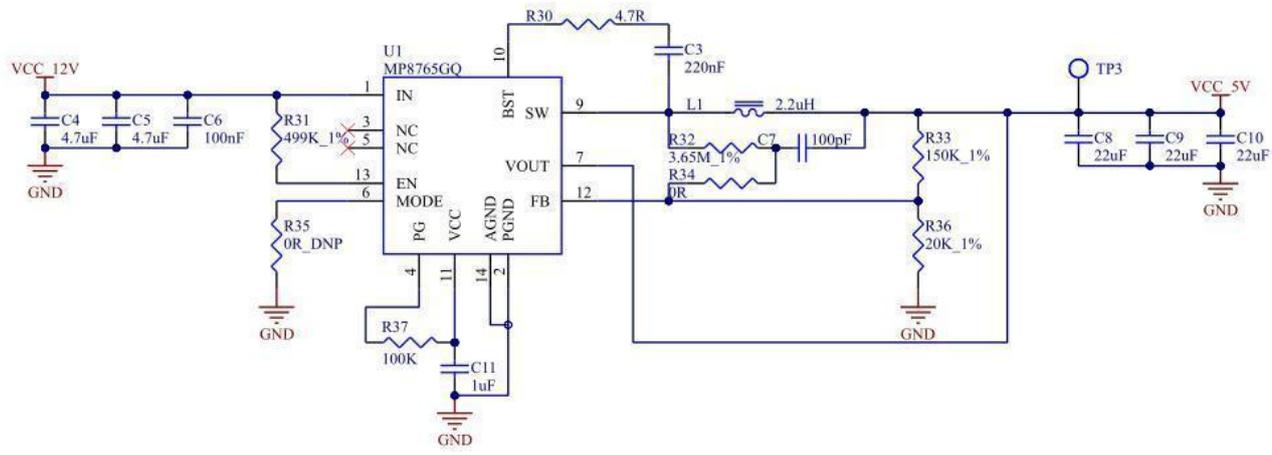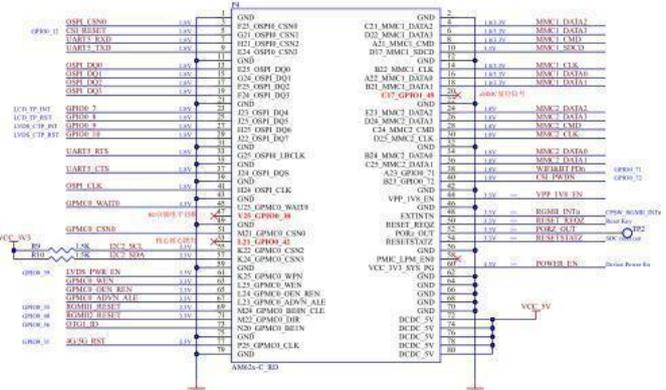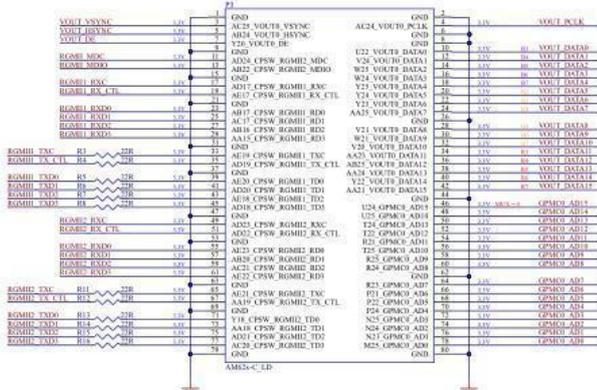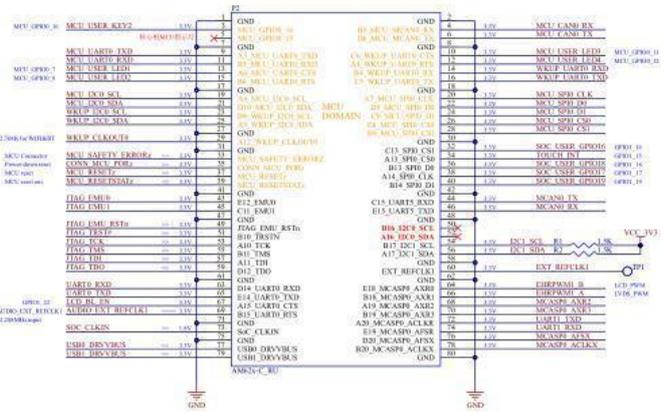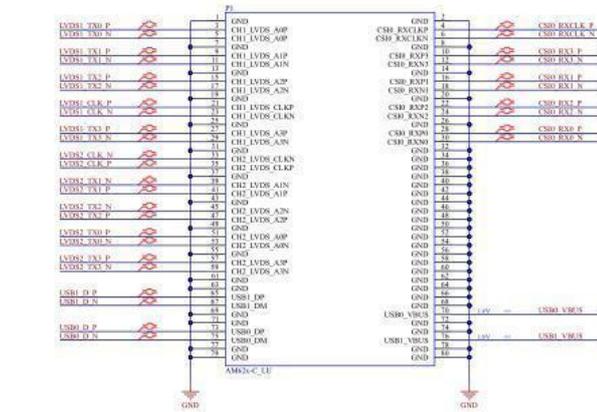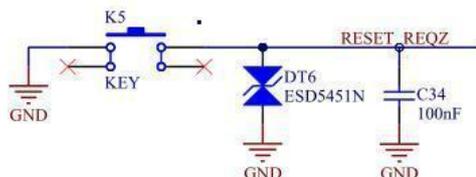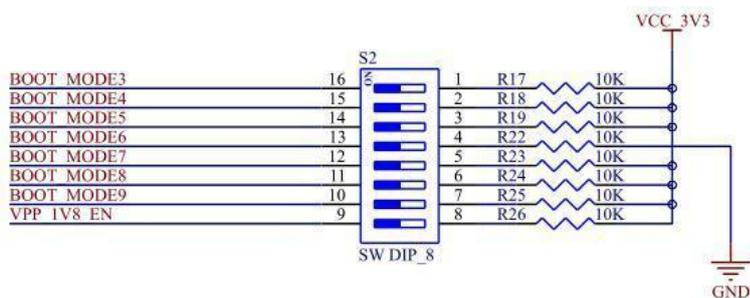
RESET KEY
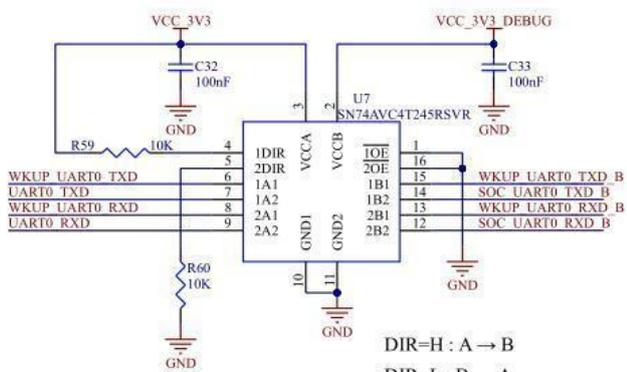
DIR=H : A → B

DIR=L : B → A

OE=H : A and B → Hi-Z

DEBUG-TYPC-C

TF-CARD
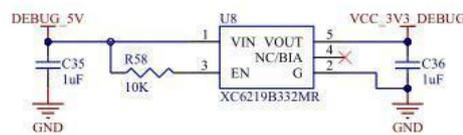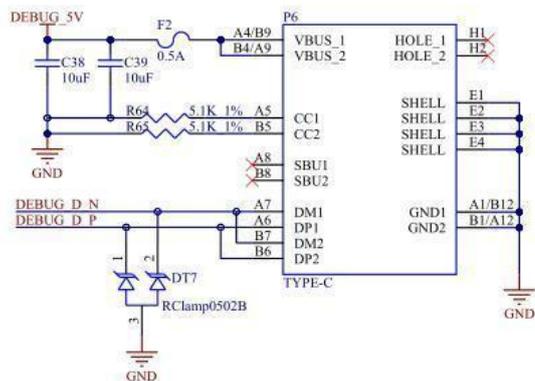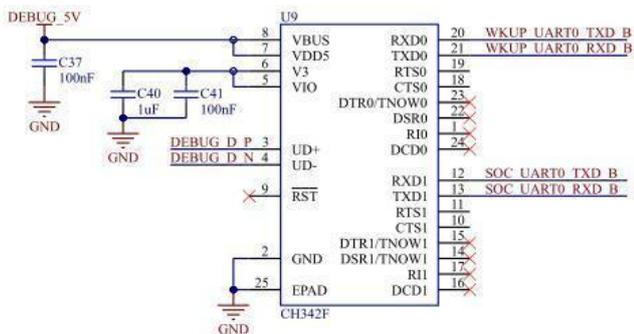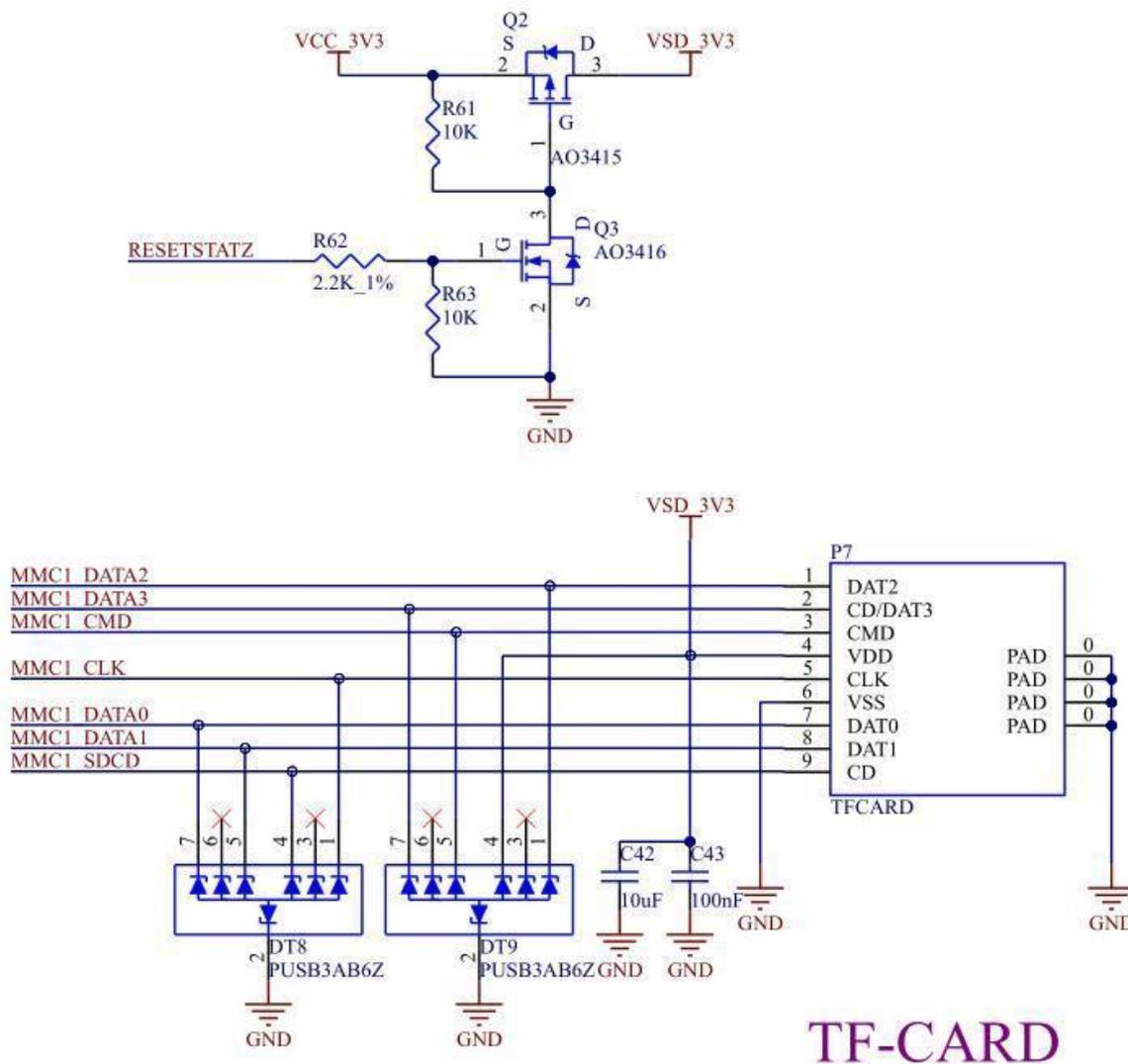
The minimum system contains SoM power, OS flashing circuit and serial debug circuit.